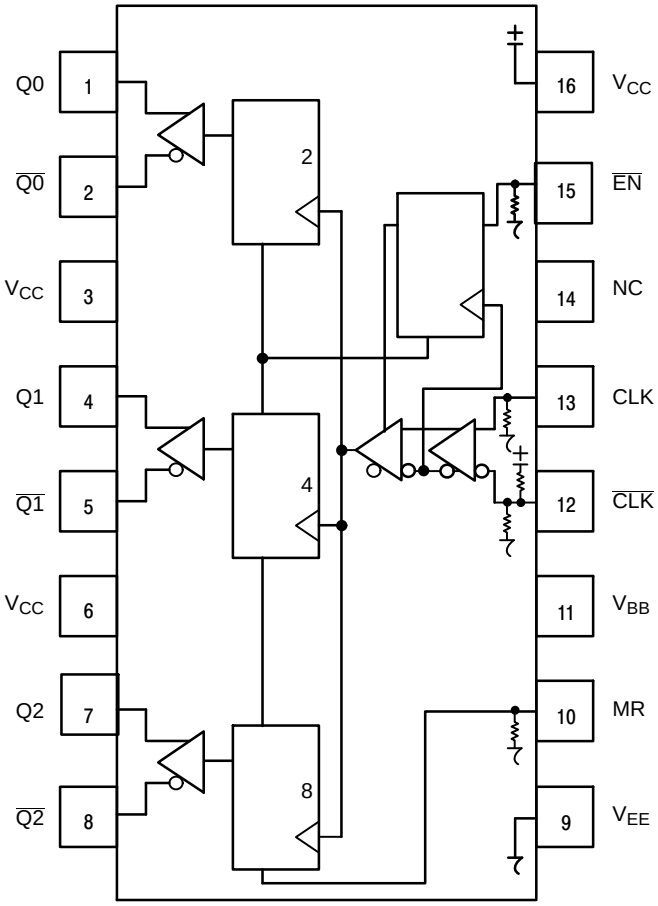
2.5 V/3.3 V ECL 2, 4, 8 Clock Generation Chip

MC100LVEP34

Description

The MC100LVEP34 is a low skew 2, 4, 8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single−ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The common enable ($\overline{EN}$) is synchronous so that the internal



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 16−Lead Pinout (Top View) **and Logic Diagram**

Table 1. PIN DESCRIPTION

Pin	Function
CLK*, $\overline{CLK}$**	ECL Diff Clock Inputs
EN*	ECL Sync Enable
MR*	ECL Master Reset
Q0, $\overline{Q0}$	ECL Diff 2 Outputs
Q1, $\overline{Q1}$	ECL Diff 4 Outputs
Q2, $\overline{Q2}$	ECL Diff 8 Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

* Pins will default LOW when left open.
**Pins will default to $V_{CC}/2$ when left open.

Table 2. FUNCTION TABLE

CLK	$\overline{EN}$	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q_{0-3}
X	X	H	Reset Q_{0-3}

Z = Low−to−High Transition
ZZ = High−to−Low Transition

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	37.5 kΩ
ESD Protection Human Body Model Machine Model Charged Device Model	 > 2 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V−O @ 0.125 in
Transistor Count	210 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

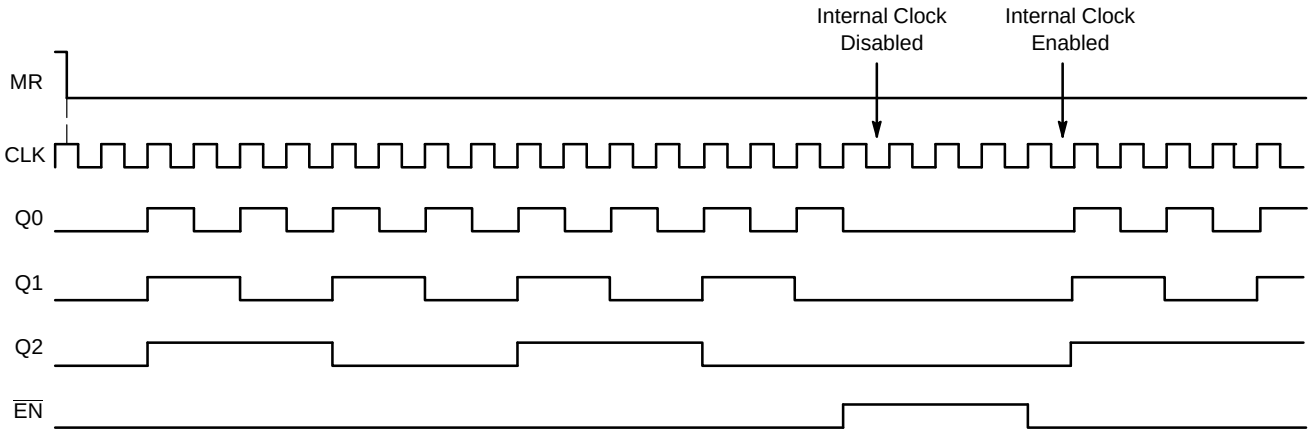
Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit

Table 5. 100EP DC CHARACTERISTICS, PECL V_{CC} = 2.5 V, V_{EE} = 0 V (Note 2)

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	40	50	60	40	50	60	42	52	62	mA
V_{OH}	Output HIGH Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{OL}	Output LOW Voltage (Note 3)	505	680	900	505	680	900	505	680	900	mV
V_{IH}	Input HIGH Voltage (Single−Ended) (Note 4)	1335		1620	1335		1620	1275		1620	mV
V_{IL}	Input LOW Voltage (Single−Ended) (Note 4)	505		900	505		900	505		900	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Diffe4.09.e 254.494 61sx1 .9070 0 8 105.4488 585.2977 Tm-0023 Tc.027.5402 Tm-0019 Tc.005O8091 .9071 refB8 0 0 8 105.4488 585										

There are two distinct functional relationships between the Master Reset and Clock:



CASE 1: If the MR is de−asserted (H−L), while the Clock is still high, the outputs will follow the second ensuing clock rising edge.

The $\overline{EN}$ signal will “freeze” the internal divider flip−flops on the first falling edge of CLK after its assertion. The internal divider flip−flops will maintain their state during the freeze. When $\overline{EN}$ is deasserted (LOW), and after the next falling edge of CLK, then the internal divider flip−flops will “unfreeze” and continue to their next state count with proper phase relationships.

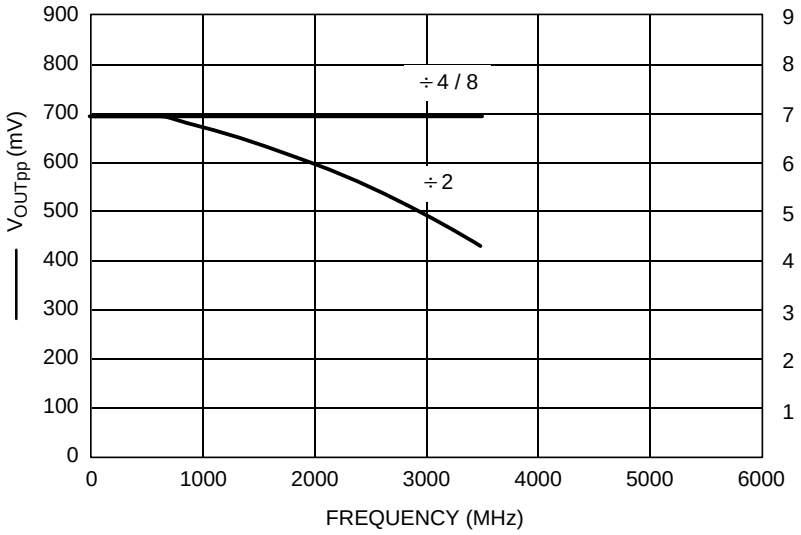


Figure 4. F_{max}

Figure 5. Typical Termination for Output Driver and Device Evaluation

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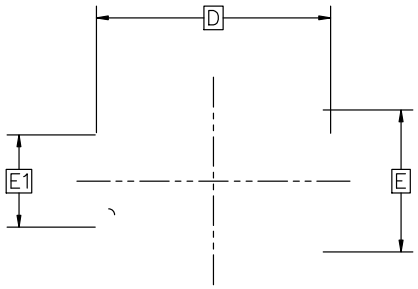
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.1[illegible]

nm TOTAL IN EXCESS OF THE

b DIMENSION AT MAXIMUM MATE



TOP VIEW

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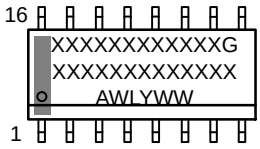
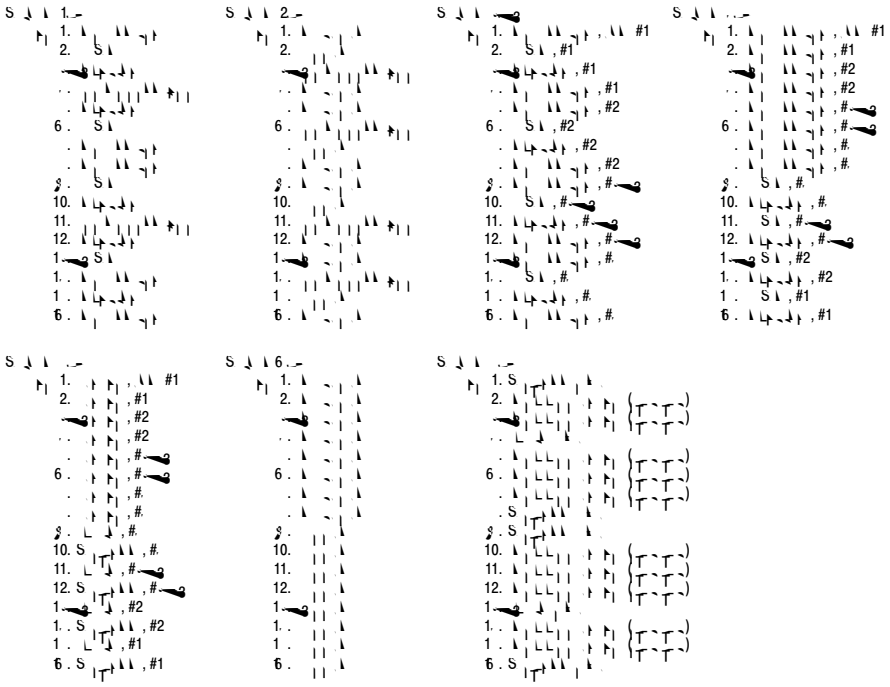
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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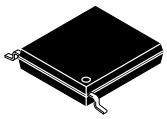

SCALE 2:1

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