

5 **2-** **D**
A D / A D
10 05, 100 05



SOIC-8
D SUFFIX
CASE 751-07

Description

The MC10EL/100EL05 is a 2-input differential AND/NAND gate. The device is functionally equivalent to the E404 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E404, the EL05 is ideally suited for those applications which require the ultimate in AC performance.

Because a negative 2-input NAND is equivalent to a 2-input OR function, the differential inputs and outputs of the device allows the EL05 to also be used as a 2-input differential OR/NOR gate.

The differential inputs employ clamp circuitry so that under open input conditions (pulled down to V_{EE}) the input to the AND gate will be HIGH. In this way, if one set of inputs is open, the gate will remain active to the other input.

The 100 Series contains temperature compensation.

Features

275 ps Propagation Delay

ESD Protection:

- > 1 kV Human Body Model,
- > 100 V Machine Model

PECL Mode Operating Range:

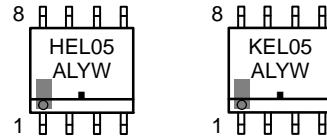
$V_{CC} = 4.2\text{ V to } 5.7\text{ V}$ with $V_{EE} = 0\text{ V}$

NECL Mode Operating Range, Emission Immunity Rating 94 V

Transistor Count = 44 devices

These Devices are Pb-Free, Halogen Free and are RoHS Compliant

MARKING DIAGRAM



- H = MC10
- K = MC100
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping†
MC10EL05DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 1)

MC100EL05DG	SOIC-8 (Pb-Free)	98 Units / Tube
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†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

MC10EL05, MC100EL05

Table 1. TRUTH TABLE

D0	D1	$\overline{D0}$	$\overline{D1}$	Q	\overline{Q}
L	L	H	H	L	H
L	H	H	L	L	H
H	L	L	H	L	H
H	H	L	L	H	L

Table 2. PIN DESCRIPTION

PIN	Function
D0, $\overline{D0}$; D1, $\overline{D1}$	

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Table 4. 10EL SERIES PECL DC CHARACTERISTICS ($V_{CC}= 5.0\text{ V}$; $V_{EE}= 0.0\text{ V}$ (Note 5))

Symbol	Characteristic	-40 C		25 C	85 C	
		Min	Typ ²⁵			

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Table 8. AC CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$; $V_{EE} = 0\text{ V}$ or $V_{CC} = 0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{\max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	135	260	440	185	275	390	215	305	420	ps
V_{PP}	Input Swing (Note 2)	150		1000	150		1000	150		1000	mV
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

- 10 Series: V_{EE} can vary +0.25 V / -0.5 V.
100 Series: V_{EE} can vary +0.8 V / -0.5 V.
- $V_{PP(\min)}$ is minimum input swing for which AC parameters guaranteed. The device has a DC gain of 40.

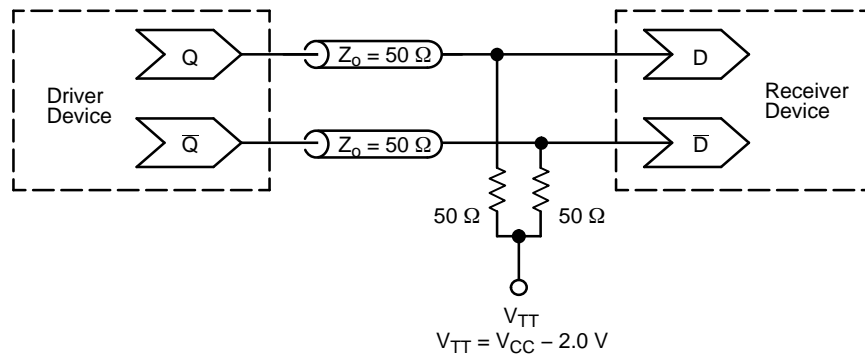


Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

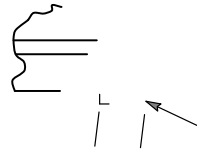
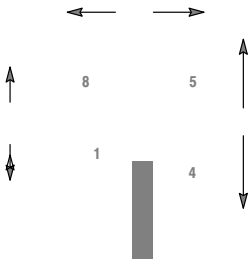
Resource Reference of Application Notes

- AN1405/D – ECL Clock Distribution Techniques
- AN1406/D – Designing with PECL (ECL at +5.0 V)
- AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D – Metastability and the ECLinPS Family
- AN1568/D – Interfacing Between LVDS and ECL
- AN1672/D – The ECL Translator Guide
- AND8001/D – Odd Number Counters Design
- AND8002/D – Marking and Date Codes
- AND8020/D – Termination of ECL Logic Devices
- AND8066/D – Interfacing with ECLinPS
- AND8090/D – AC Characteristics of ECL Devices

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SEATING
PLANE



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