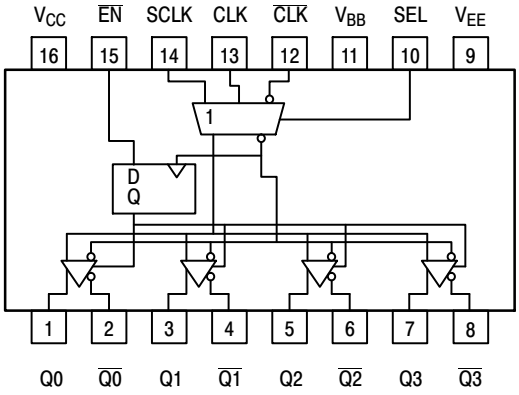


CLK, $\overline{\text{CLK}}$ ECL Diff Clock Inputs

V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		8	V
I_{out}	Output Current	Continuous Surge		50 100	mA
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 6	V
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			40 to +85	°C
T_{stg}	Storage Temperature Range			65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC 16	130 75	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC 16	33 to 36	°C/W
T_{sol}	Wave Solder (Pb-Free)	<2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

(V_{CC} = 5.0 V; V_{EE} = 0.0 V (Note 1))

		– °			°			°			
I_{EE}	Power Supply Current		25	35		25	35		25	35	mA
V_{OH}	Output HIGH Voltage (Note 2)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3050		3500	3050		3520	3050		3555	mV
V_{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.06 V / 0.5 V.

(V_{CC} = 0 V; V_{EE} = 5.0 V (Note 1))

		– °			°			°			
I_{EE}	Power Supply Current		25	35		25	35		25	35	mA
V_{OH}	Output HIGH Voltage (Note 2)	1080	990	890	980	895	810	910	815	720	mV
V_{OL}	Output LOW Voltage (Note 2)	1950	1800	1650	1950	1790	1630	1950	1773	1595	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	1230		890	1130		810	1060		720	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1950		1500	1950		1480	1950		1445	mV
V_{BB}	Output Voltage Reference	1.43		1.30	1.35		1.25	1.31		1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	2.5		0.4	2.5		0.4	2.5		0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

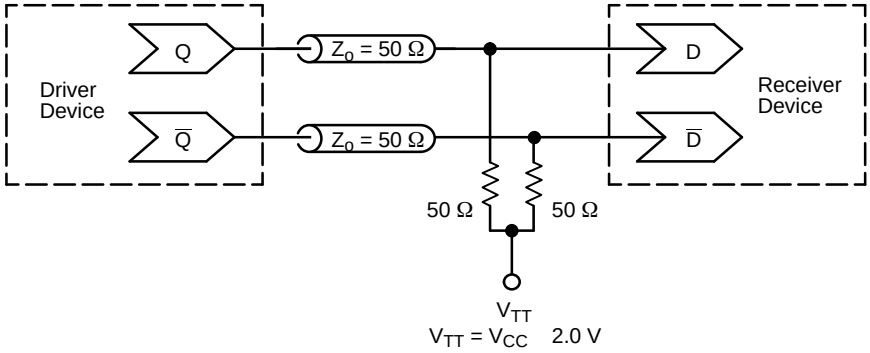
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.06 V / −0.5 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} 2.0 V.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

(V_{CC} = 5.0 V; V_{EE} = 0.0 V (Note 1))

		– °			°			°			
I_{EE}	Power Supply Current		25	35		25	35		25	38	mA
V_{OH}	Output HIGH Voltage (Note 2)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150							

(V_{CC} = 0 V; V_{EE} = 5.0 V (Note 1))

		– °			°			°			
I_{EE}	Power Supply Current		25	35		25	35		25	38	mA
V_{OH}	Output HIGH Voltage (Note 2)	1085	1005	880	1025	955	880	1025	955	880	mV
V_{OL}	Output LOW Voltage (Note 2)	1830	1695	1555	1810	1705					



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ECL Clock Distribution Techniques

Designing with PECL (ECL at +5.0 V)

ECLinPS™ I/O SPiCE Modeling Kit

Metastability and the ECLinPS Family

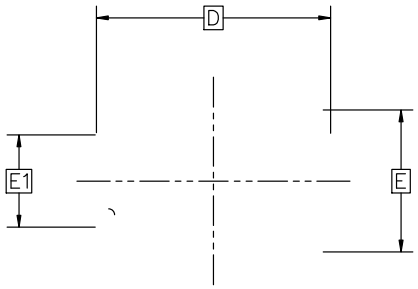
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.1[illegible]

nm TOTAL IN EXCESS OF THE

b DIMENSION AT MAXIMUM MATE

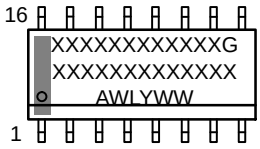


TOP VIEW

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

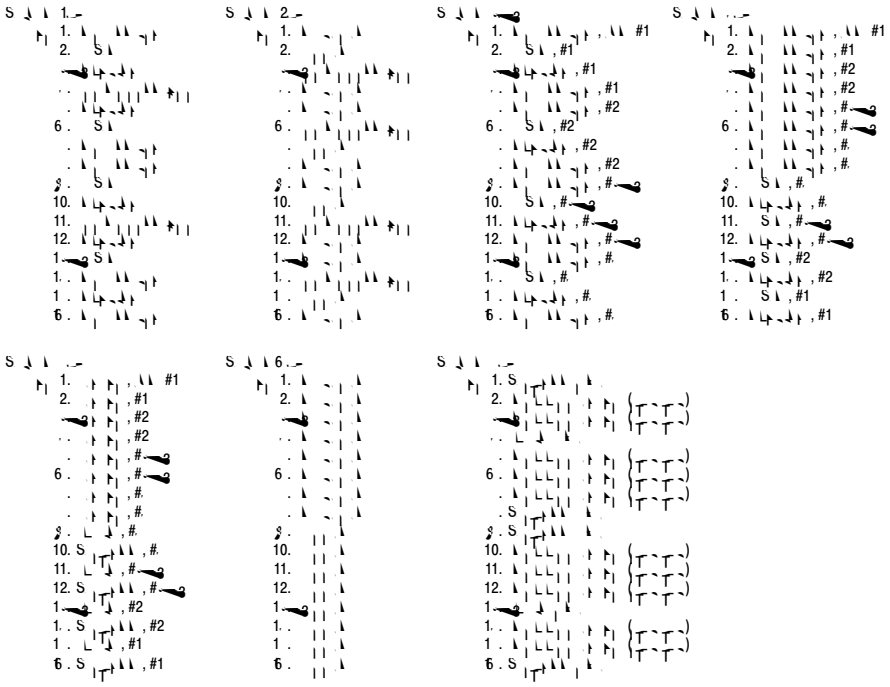
DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 2 OF 2**