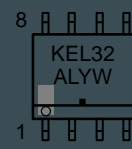


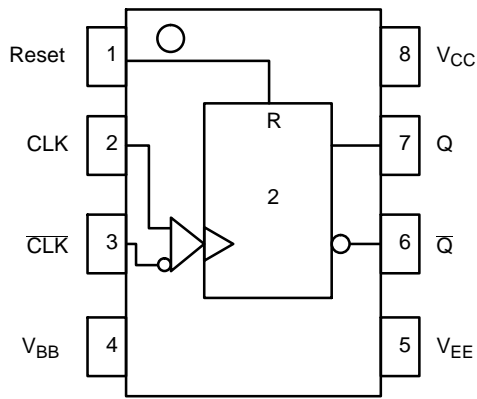
5 | **2** | **r**
10 | **32** | **100** | **32**



The MC10EL100EL32 is an integrated 2 divider. The differential clock inputs and the V_{BB} allow a differential, single-ended or AC coupled interface to the device. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} an(840.3(9B8(decouple)TJ-5.2271 -1no0J12.2271 -CCBB)T]0 0 10 115)-40.310 115)-40.310 15A82c-.00310Tw(anv).8(di)3505(a a 0).4(



- 510 ps Propagation Delay
- 3.0 GHz Toggle Frequency
- ESD Protection:
 - > 1 kV Human Body Model
 - > 100 V Machine Model
- PECL Mode Operating Range:
 - $V_{CC} = 4.2 \text{ V to } 5.7 \text{ V}$ with $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:
 - $V_{CC} = 0 \text{ V}$ with $V_{EE} = 4.2 \text{ V to } 5.7 \text{ V}$
- Internal Input Pulldown Resistors on CLK(s) and R.
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity
 - Level 1 for SOIC 8 NB
- For Additional Information, see Application Note [AND8003/D](#)
- Flammability Rating: UL 94 V 0 @ 0.125 in,
- Oxygen Index: 28 to 34
- Transistor Count = 82 devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



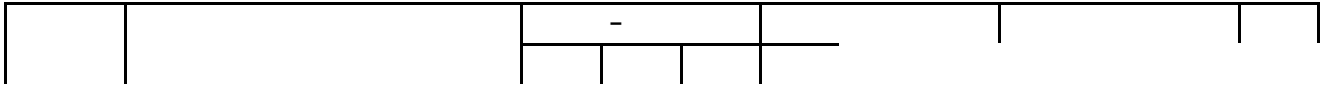
CLK, $\overline{\text{CLK}}$	ECL Clock Inputs*
Reset	ECL Asynch Reset*
Q, $\overline{\text{Q}}$	ECL Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

*Pins will default low when left open.

V_{CC}	PECL Mode Power Supply	$V_{\text{EE}} = 0 \text{ V}$		8	V
V_{EE}	NECL Mode Power Supply	$V_{\text{CC}} = 0 \text{ V}$		8	V
V_{I}	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{\text{EE}} = 0 \text{ V}$ $V_{\text{CC}} = 0 \text{ V}$	$V_{\text{I}} \quad V_{\text{CC}}$ $V_{\text{I}} \quad V_{\text{EE}}$	6 6	V
I_{out}	Output Current	Continuous Surge		50 100	mA
I_{BB}	V_{BB} Sink/Source			0.5	mA
T_{A}	Operating Temperature Range			40 to +85	C
T_{stg}	Storage Temperature Range			65 to +150	C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC 8 NB	190 130	C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC 8 NB	41 to 44	C/W
T_{sol}	Wave Solder (Pb-Free)	<2 to 3 sec @ 260 C		265	C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

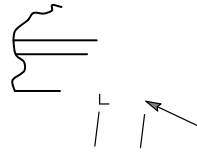
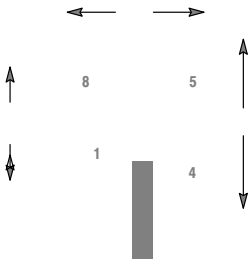
($V_{CC} = 5.0\text{ V}$; $V_{EE} = 0\text{ V}$ or $V_{CC} = 0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))



ECL Clock Distribution Techniques
Designing with PECL (ECL at +5.0 V)
ECLinPS™ I/O SPiCE Modeling Kit
Metastability and the ECLinPS Family
Interfacing Between LVDS and ECL
The ECL Translator Guide
Odd Number Counters Design
Marking and Date Codes
Termination of ECL Logic Devices
Interfacing with ECLinPS
AC Characteristics of ECL Devices

SOIC 8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



SEATING
PLANE



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