5 E ÷2, ÷4, ÷ lo k o

10E 34, 100E 34

Description

The MC10/100EL34 is a low skew ÷2, ÷4, ÷8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The common enable ($\overline{EN}$) is synchronous so that the internal

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Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−8	V
V_I					

Table 8. 100EL SERIES NECL DC CHARACTERISTICS (V_{CC} = 0 V; V_{EE} = −5.0 V (Note 1))

Symbol	Characteristic	40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			39			39			42	mA
V_{OH}	Output HIGH Voltage (Note 2)	−1085	−1005	−880	−1025	−955	−880	−1025	−955	−880	mV
V_{OL}	Output LOW Voltage (Note 2)	−1830	−1695	−1555	−1810	−1705	−1620	−1810	−1705	−1620	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	−1165		−880	−1165		−880	−1165		−880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	−1810		−1475	−1810		−1475	−1810		−1475	mV
V_{BB}	Output Voltage Reference	−1.38		−1.26	−1.38		−1.26	−1.38		−1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	−2.8		−0.4	−2.8		−0.4	−2.8		−0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / −0.5 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

Table 9. AC CHARACTERISTICS (V_{CC} = 5.0 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = −5.0 V (Note 1))

Symbol	Characteristic	40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
fmax	Maximum Toggle Frequency	1.1			1.1			1.1			GHz
t_{PLH} t_{PHL}	Propagation CLK to Q0 Delay to CLK to Q1,2 Output MR to Q	960 900 750		1200 1140 1060	960 900 750		1200 1140 1060	970 910 790		1210 1150 1090	ps
t_{SKEW}	Within-Device Skew (Note 2)		100			100			100		ps
t_{JITTER}	Cycle-to-Cycle Jitter		1.0			1.0			1.0		ps
t_S	Setup Time $\overline{EN}$	400			400			400			ps
t_H	Hold Time $\overline{EN}$	250			250			250			ps
t_{RR}	Set/Reset Recovery	400	200		400	200		400	200		ps
V_{PP}	Input Swing (Note 3)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	225		475	225		475	225		475	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. 10 Series: V_{EE} can vary +0.06 V / −0.5 V.
   100 Series: V_{EE} can vary +0.8 V / −0.5 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. V_{PP}min is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

There are two distinct functional relationships between the Master Reset and Clock:

CASE 1: If the MR is De-asserted (H L), While the Clock is Still High, the Outputs will Follow the First Ensuing Clock Rising Edge.

CASE 2: If the MR is De asserted (H L), After the Clock has Transitioned Low, the

The $\overline{EN}$ signal will “freeze” the internal divider flip flops on the first falling edge of CLK after its assertion. The internal divider flip flops will maintain their state during the freeze. The $\overline{EN}$ is deasserted (LOW), and after the next falling edge of CLK, then the internal divider flip flops will “unfreeze” and continue to their next state count with proper phase relationships.

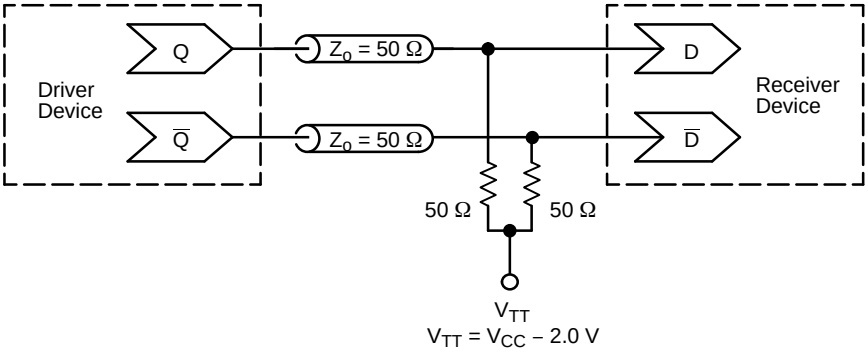

Figure 4. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

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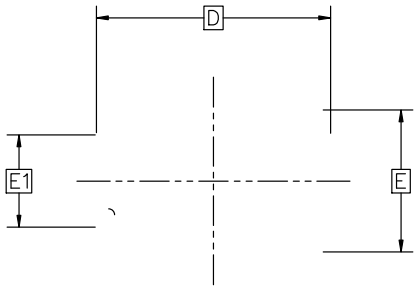
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.1[illegible]

nm TOTAL IN EXCESS OF THE

b DIMENSION AT MAXIMUM MATE



TOP VIEW

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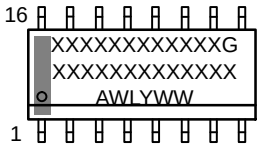
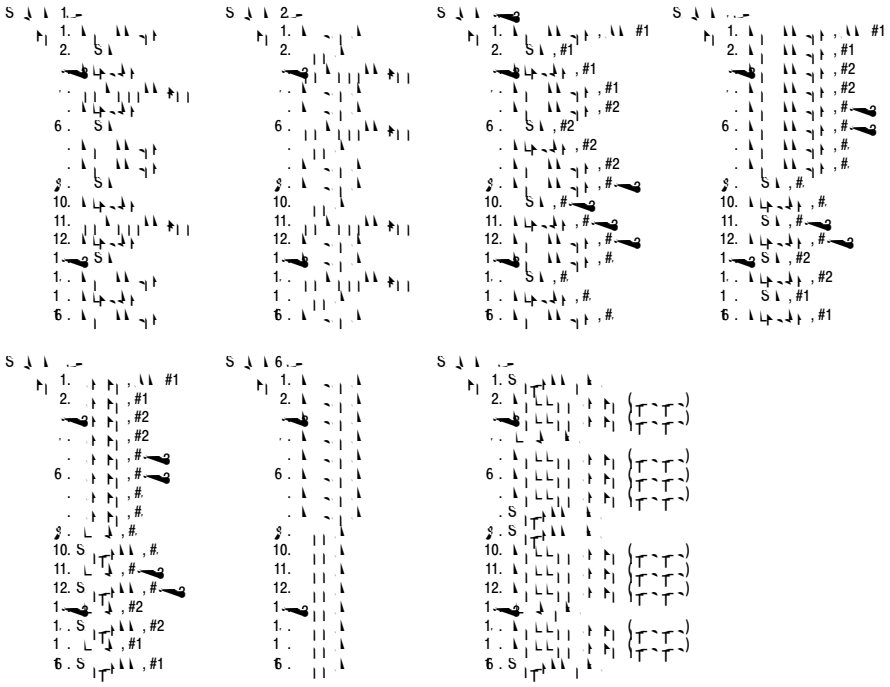
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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