

5 E ÷2, ÷4, ÷8 b k o 10E 34, 100E 34

Description

The MC10/100EL34 is a low skew ÷2, ÷4, ÷8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The common enable (\overline{EN}) is synchronous so that the internal

MC10EL34, MC100EL34

Table 4. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|----------|------------------------|-----------------------|-------------|--------|------|
| V_{CC} | PECL Mode Power Supply | $V_{EE} = 0\text{ V}$ | | 8 | V |
| V_{EE} | NECL Mode Power Supply | $V_{CC} = 0\text{ V}$ | | -8 | V |
| V_I | | | | | |

MC10EL34, MC100EL34

Table 8. 100EL SERIES NECL DC CHARACTERISTICS ($V_{CC} = 0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

| Symbol | Characteristic | 40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | | 39 | | | 39 | | | 42 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | -1085 | -1005 | -880 | -1025 | -955 | -880 | -1025 | -955 | -880 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | -1830 | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1165 | | -880 | -1165 | | -880 | -1165 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1810 | | -1475 | -1810 | | -1475 | -1810 | | -1475 | mV |
| V_{BB} | Output Voltage Reference | -1.38 | | -1.26 | -1.38 | | -1.26 | -1.38 | | -1.26 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3) | -2.8 | | -0.4 | -2.8 | | -0.4 | -2.8 | | -0.4 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0\text{ V}$.
3. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1 V.

Table 9. AC CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CC} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

| Symbol | Characteristic | 40°C | | | 25°C | | | 85°C | | | Unit |
|------------------------|---|------|-----|------|------|-----|------|------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Toggle Frequency | 1.1 | | | 1.1 | | | 1.1 | | | GHz |
| t_{PLH} t_{PHL} | Propagation CLK to Q0 | 960 | | 1200 | 960 | | 1200 | 970 | | 1210 | ps |
| | Delay to CLK to Q1,2 | 900 | | 1140 | 900 | | 1140 | 910 | | 1150 | |
| | Output MR to Q | 750 | | 1060 | 750 | | 1060 | 790 | | 1090 | |
| t_{SKEW} | Within-Device Skew (Note 2) | | 100 | | | 100 | | | 100 | | ps |
| t_{JITTER} | Cycle-to-Cycle Jitter | | 1.0 | | | 1.0 | | | 1.0 | | ps |
| t_S | Setup Time \overline{EN} | 400 | | | 400 | | | 400 | | | ps |
| t_H | Hold Time \overline{EN} | 250 | | | 250 | | | 250 | | | ps |
| t_{RR} | Set/Reset Recovery | 400 | 200 | | 400 | 200 | | 400 | 200 | | ps |
| V_{PP} | Input Swing (Note 3) | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | mV |
| t_r t_f | Output Rise/Fall Times Q (20% - 80%) | 225 | | 475 | 225 | | 475 | 225 | | 475 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. 10 Series: V_{EE} can vary +0.06 V / -0.5 V.
100 Series: V_{EE} can vary +0.8 V / -0.5 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. V_{ppmin} is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈ 40 .

MC10EL34, MC100EL34

There are two distinct functional relationships between the Master Reset and Clock:

CASE 1: If the MR is De-asserted (H L), While the Clock is Still High, the Outputs will Follow the First Ensuing Clock Rising Edge.

CASE 2: If the MR is De-asserted (H L), After the CLK has Transitioned Low, the

The \overline{EN} signal will “freeze” the internal divider flip flops on the first falling edge of CLK after its assertion. The internal divider flip flops will maintain their state during the freeze. The \overline{EN} is deasserted (LOW), and after the next falling edge of CLK, then the internal divider flip flops will “unfreeze” and continue to their next state count with proper phase relationships.

MC10EL34, MC100EL34

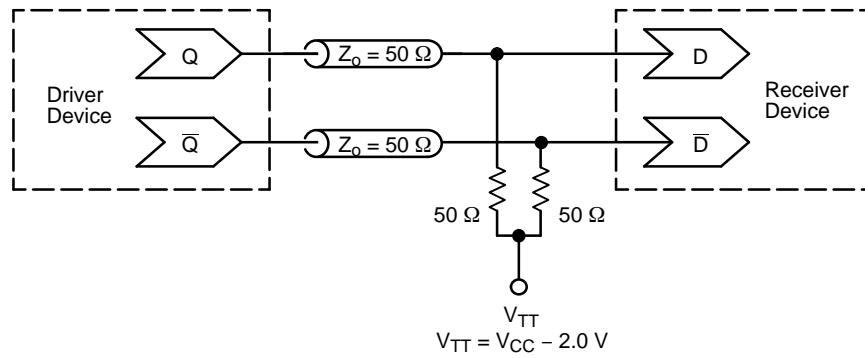


Figure 4. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) Termination of ECL Logic Devices.)

Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

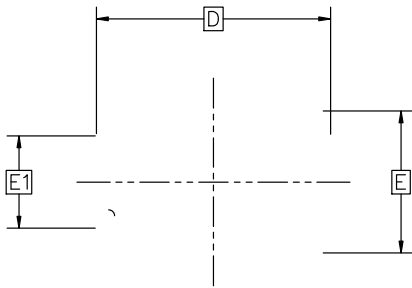


SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

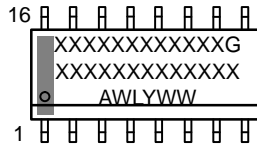
- 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.1 ϕ

b DIMENSION AT MAXIMUM MATE nm TOTAL IN EXCESS OF THE



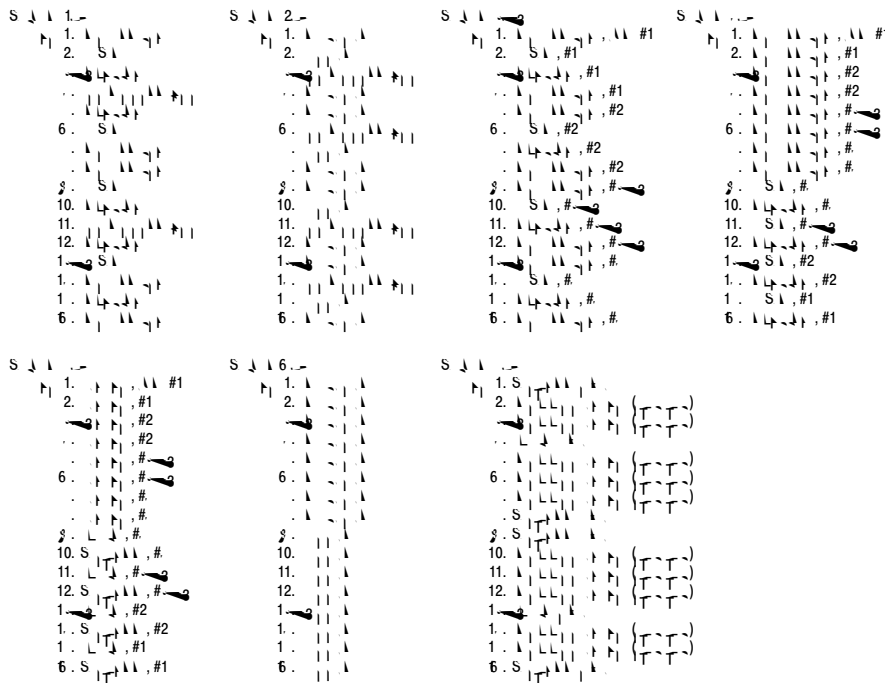
TOP VIEW

**GENERIC
MARKING DIAGRAM***



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



| | | |
|-------------------------|-------------------------------------|---|
| DOCUMENT NUMBER: | 98ASB42566B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOIC-16 9.90X3.90X1.37 1.27P | PAGE 2 OF 2 |

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**
