5 V
o k - o
10 5ϟ, 100 5ϟ

SOIC −8 NB
D SUFFIX
CASE 751−07

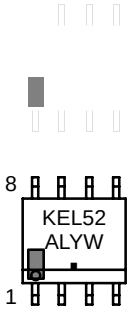
Description

The MC10EL/100EL52 is a differential data, differential clock D flip-flop with reset. The device is functionally equivalent to the E452 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E452, the EL52 is ideally suited for those applications which require the ultimate in AC performance.

Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EL52 allow the device to also be used as a negative edge triggered device.

The EL52 employs input clamping circuitry so that under open input conditions (pulled down to V_{EE}) the outputs of the device will remain stable.

The 100 Series contains temperature compensation.



Features

- 365 ps Propagation Delay
- 2.0 GHz Toggle Frequency
- ESD Protection:
  - > 1 kV Human Body Model
  - > 100 V Machine Model
- PECL Mode Operating Range
- For additional marking information, refer to Application Note AND8002/D
- MARKING DIAGRAM

Table 4. 10EL SERIES PECL DC CHARACTERISTICS (V_{CC} = 5.0 V; V_{EE} = 0 V (Note 2))

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		21	25		21	25		21	25	mA
V_{OH}	Output HIGH Voltage (Note 2)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 3)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3050		3500	3050		3520	3050		3555	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) D CLK	 3.4 2.5		 4.6 4.4	 3.4 2.5		 4.6 4.4	 3.4 2.5		 4.6 4.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. Input and output parameters vary 1:1 with V_{CC}.
   V_{EE} can vary +0.25 V / −0.5 V for +25 C and +85 C. or V_{EE} can vary +0.06 V / −0.5 V for −40 C.
3. Outputs are terminated through a 50 ohm resistor to V_{CC} − 2.0 V.
4. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

Table 5. 10EL SERIES NECL DC CHARACTERISTICS (V_{CC} = 0 V; V_{EE} = −5.0 V (Note 1))

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		21	25		21	25		21	25	mA
V_{OH}	Output HIGH Voltage (Note 2)	−1080	−990	−890	−980	−895	−810	−910	−815	−720	mV
V_{OL}	Output LOW Voltage (Note 2)	−1950	−1800	−1650	−						

Table 6. 100EL SERIES PECL DC CHARACTERISTICS (V_{CC} = 5.0 V; V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		21	25		21	25		24	29	mA
V_{OH}	Output HIGH Voltage (Note 2)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV

V

Table 8. AC CHARACTERISTICS (V_{CC} = 5.0 V; V_{EE} = 0 V or V_{CC} = 0 V; V_{EE} = −5.0 V (Note 1))

		−40 C			25 C			85 C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
fmax	Maximum Toggle Frequency	1.8	2.5		2.2	2.8		2.2	2.8		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK	225	335	515	275						

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques

AN1406/D − Designing with PECL (ECL at +5.0 V)

AN1503/D − ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D − Metastability and the ECLinPS Family

AN1568/D − Interfacing Between LVDS and ECL

AN1672/D − The ECL Translator Guide

AND8001/D − Odd Number Counters Design

AND8002/D − Marking and Date Codes

AND8020/D − Termination of ECL Logic Devices

AND8066/D − Interfacing with ECLinPS

AND8090/D − AC Characteristics of ECL Devices

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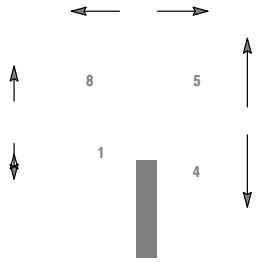
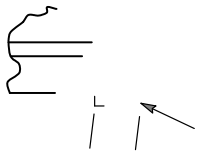
DATE 16 FEB 2011





SEATING
PLANE