

3.3 V/5 V ECL 4-Input OR/NOR

MC10EP01, MC100EP01

Description

The MC10EP01 and MC100EP01 are 4-input ECL OR/NOR gates with 3.3 V and 5 V supply voltages. They are available in 16-pin SOIC and 16-pin SSOP packages. The MC10EP01 is a 3.3 V device and the MC100EP01 is a 5 V device. Both devices are available in both standard and low-power versions. The low-power versions are designed for applications where power consumption is a concern. The standard versions are designed for applications where performance is a concern. The low-power versions have a typical propagation delay of 1.3 ns and a typical power dissipation of 10 mW. The standard versions have a typical propagation delay of 1.0 ns and a typical power dissipation of 15 mW. Both devices are available in both standard and low-power versions. The low-power versions are designed for applications where power consumption is a concern. The standard versions are designed for applications where performance is a concern. The low-power versions have a typical propagation delay of 1.3 ns and a typical power dissipation of 10 mW. The standard versions have a typical propagation delay of 1.0 ns and a typical power dissipation of 15 mW.

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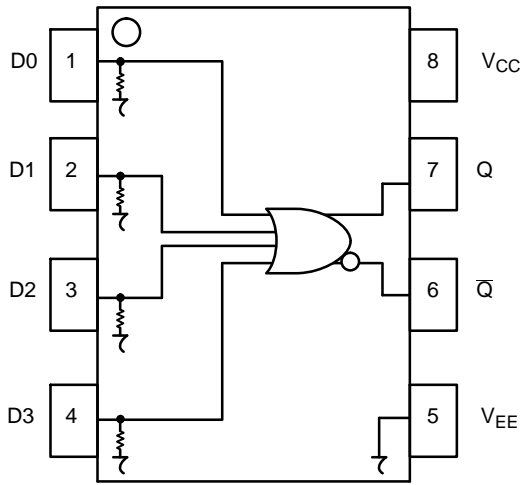


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Function
D0 – D3	ECL Data Inputs
Q, Q̄	ECL Data Outputs
V _{CC}	Positive Supply
V _{EE}	Negative Supply
EP	

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Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		6	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	V_I V_{CC} V_I V_{EE}	6 -6	V
I_{out}	Output Current	Continuous Surge		50 100	mA
I_{BB}	V_{BB} Sink/Source			0.5	mA
T_A	Operating Temperature Range			-40 to +85	C
T_{stg}	Storage Temperature Range			-65 to +150	C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 NB SOIC-8 NB	190 130	C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8 NB	41 to 44	C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44	C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	C/W
T_{sol}	Wave Solder (Pb-Free)	< 2 to 3 sec @ 260 C		265	C
θ_{JC}	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

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Table 5. 10EP DC CHARACTERISTICS, PECL ($V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 1))

Symbol	Characteristic	-40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	20	24	31	20	24	31	20	24	31	mA
V_{OH}											

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Table 11. AC CHARACTERISTICS ($V_{CC} = 3.0\text{ V to }5.5\text{ V}$; $V_{EE} = 0\text{ V or }V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V to }-5.5\text{ V}$ (Note 1))

Symbol	Characteristic	-40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 2. $F_{max}/JITTER$)		> 3			> 3			> 3		GHz

t_{PLH} .

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Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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