

# 3.3 V/5 V ECL 2-Input Differential XOR/XNOR

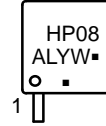
## MC10EP08, MC100EP08



SOIC-8 NB  
 D SUFFIX  
 CASE 751-07

TSSOP-8  
 DT SUFFIX  
 CASE 948R-02

### MARKING DIAGRAM



### Description

The MC10/100EP08 is a differential XOR/XNOR gate. The EP08 is ideal for applications requiring the fastest AC performance available. The 100 Series contains temperature compensation.

### Features

- 250 ps Typical Propagation Delay
- Maximum Frequency = > 3 GHz Typical
- PECL Mode Operating Range:  
 $V_{CC} = 3.0\text{ V to } 5.5\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  
 $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V to } -5.5\text{ V}$
- Open Input Default State
- Safety Clamp on Inputs
- Q Output Will Default LOW with Inputs Open or at  $V_{EE}$
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

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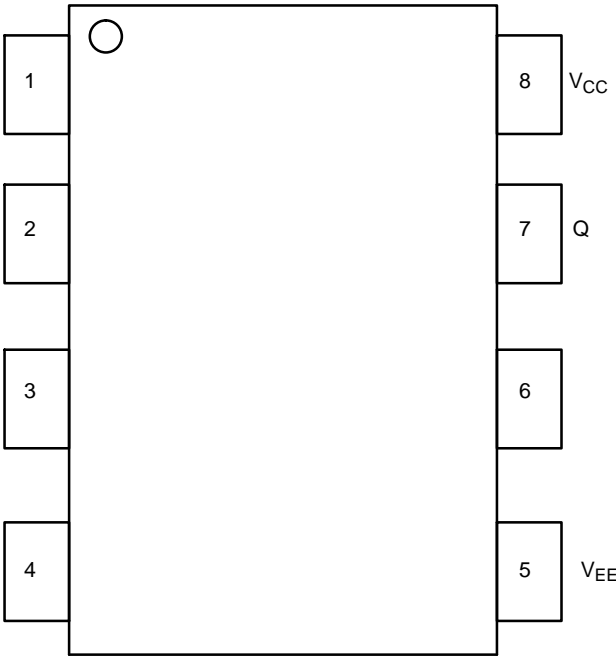


Figure 1. 8-Lead Pinout (Top View)

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**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		6	V
$V_{EE}$	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-6	V
$V_I$	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I$ $V_{CC}$ $V_I$ $V_{EE}$	6 -6	V
$I_{out}$	Output Current	Continuous Surge		50 100	mA
$T_A$	Operating Temperature Range			-40 to +85	C
$T_{stg}$	Storage Temperature Range			-65 to +150	C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 NB SOIC-8 NB	190 130	C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8 NB	41 to 44	C/W
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	C/W
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44	C/W
$T_{sol}$	Wave Solder (Pb-Free)	< 2 to 3 sec @ 260 C		265	C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 5. 10EP DC CHARACTERISTICS, PECL** ( $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	20	28	36	20	30	38	20	32	38	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
$V_{OL}$	Output LOW Voltage (Note 2)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2090		2415	2155		2480	2215		2540	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1365		1690	1430		1755	1490		1815	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	2.0		3.3	2.0		3.3	2.0		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current										$\mu\text{A}$
	$\frac{D}{\bar{D}}$	0.5 -150			0.5 -150			0.5 -150			

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.
2. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 6. 10EP DC CHARACTERISTICS, PECL** ( $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	20	28	36	20	30	38	20	32	38	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
$V_{OL}$	Output LOW Voltage (Note 2)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3790		4115	3855		4180	3915		4240	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3065		3390	3130		3455	3190		3515	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	8 65.1402 616.5355 Tm(V)Tβ.5 0 0 6.5 70.46933 Gu-.6623 Tc.0001 TwET264.0762.0.12 .90707 14.1798 ref									



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**Table 10. 100EP DC CHARACTERISTICS, NECL** ( $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 1))

Symbol	Characteristic	-40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	20	28	36	20	30	38	20	32	40	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
$V_{OL}$	Output LOW Voltage (Note 2)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	$V_{EE} + 2.0$		0.0	$V_{EE} + 2.0$		0.0	$V_{EE} + 2.0$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current D $\bar{D}$	0.5 -150			0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .
2. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ;  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 11. AC CHARACTERISTICS** ( $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 1))

Symbol	Characteristic	-40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Frequency (Figure 2)		> 3			> 3			> 3		GHz
$t_{PLH}$ , $t_{PHL}$											

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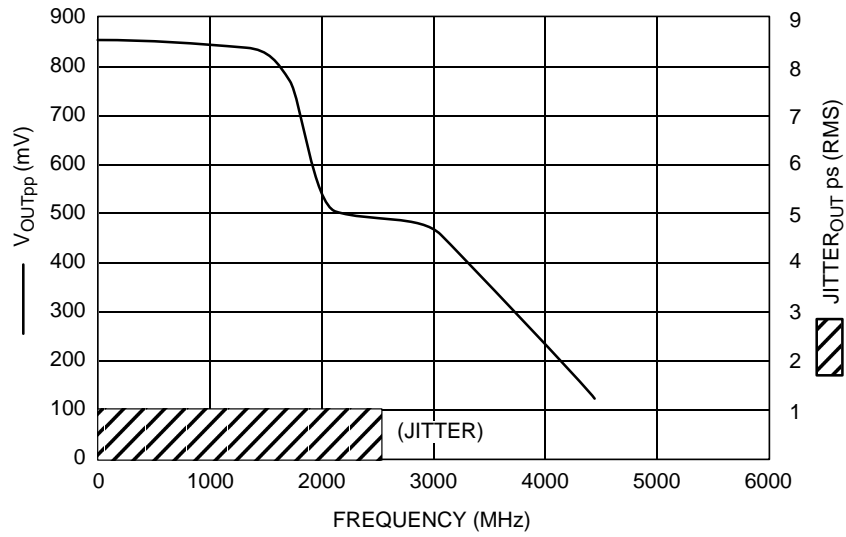


Figure 2. F<sub>max</sub>/Jitter

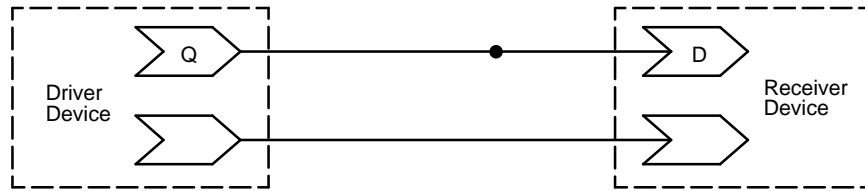


Figure 3. Typical Termination for Output Driver and Device Evaluation  
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices)

## MC10EP08, MC100EP08

### Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D –





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