3.3 /5 ECL Q D F -F D C

MC10EP131, MC100EP131

Description

The MC10/100EP131 is a Quad Master slaved D flip flop with common set and separate resets. The device is an expansion of the E131 with differential common clock and individual clock enables. With AC performance faster than the E131 device, the EP131 is ideal for applications requiring the fastest AC performance available.

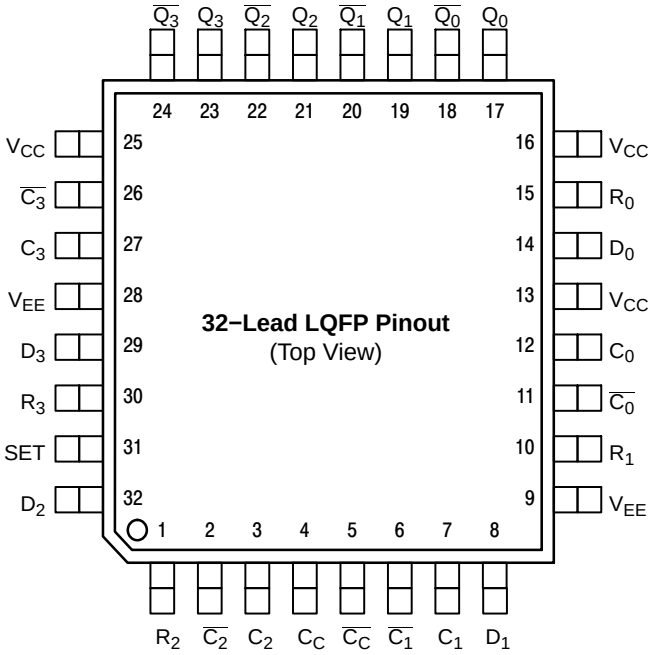
Each flip flop may be clocked separately by holding Common Clock (C_C) LOW and $\overline{C_C}$ HIGH, then using the differential Clock Enable inputs for clocking ($C_{0\ 3}$, $\overline{C_{0\ 3}}$).

Common clocking is achieved by holding the differential inputs $C_{0\ 3}$ LOW and $\overline{C_{0\ 3}}$ HIGH while using the differential Common Clock (C_C) to clock all four flip flops. When left floating open, any differential input will disable operation due to input pulldown resistors forcing an output default state.

Individual asynchronous resets ($R_{0\ 3}$) and an asynchronous set (SET) are provided.

Data enters the master when both C_C and $C_{0\ 3}$ are LOW, and transfers to the slave when either C_C or $C_{0\ 3}$ (or both) go HIGH.

clocking i031 0 TD3L 3 GHzC6ac.31(ypqui



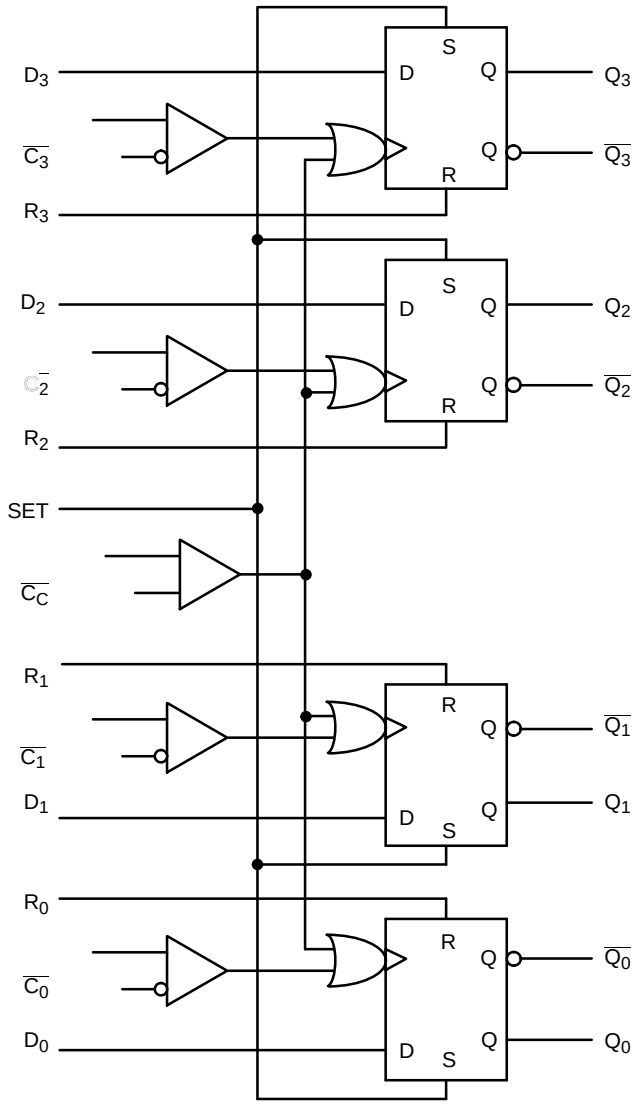


Table 1. PIN DESCRIPTION

PIN	FUNCTION
D_{0-3}*	ECL Data Inputs
C_{0-3}*, $\overline{C_{0-3}}$*	ECL Separate Clock Inputs
C_C*, $\overline{C_C}$*	ECL Common Clock Inputs
R_{0-3}*	ECL Asynchronous Reset
SET*	ECL Asynchronous Set
Q_{0-3}, $\overline{Q_{0-3}}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	 > 2 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb−Free Pkg
LQFP−32	Level 2
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V−0 @ 0.125 in
Transistor Count	935 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

Table 7. 10EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = −5.5 V to −3.0 V (Note 8)

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	70	95	120	70	95	120	70	95	120	mA
VOH	Output HIGH Voltage (Note 9)	−1135	−1010	−885	−1070	−945	−820	−1010	−885	−760	mV
V_{OL}	Output LOW Voltage (Note 9)	−1935	−1810	−1685	−1870	−1745	−1620	−1810	−1685	−1560	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	−1210		−885	−1145		−820	−1085		−760	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1935		−1610	−1870		−1545	−1810		−1485	mV
V_{IHCMR}	Input HIGH Voltage Common Mode										

Table 9. 100EP DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 14)

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	70	95	120	75	97	120	80	105	130	mA
V_{OH}	Output HIGH Voltage (Note 15)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 15)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input LOW Voltage (Single−Ended)	3055		3375	3055		3375	3055		3375	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 16)	2.0		5.0	2.0		5.0	2.0			

Table 11. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.0 V to −5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 20)

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 3. Frequency vs. V_{OUTpp} and JITTER)		> 3			> 3			> 3		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential C_C C_{0-3} R_{0-3} SET	320 320 320 300	450 450 430 430	520 520 520 550	380 400 380 380	460 500 480 460	580 600 580 580	450 450 450 400	560 560 560 530	650 650 700 650	ps
t_{RR}	Set/R0−3 Recovery	290	210		290	210		350	280		ps
t_S t_H	Setup Time Hold Time	120	80		120	80		120	80		ps
t_{PW}	Minimum Pulse Rate SET, R_{0-3}	550	400		550	400		550	400		
t_{JITTER}	Cycle−to−[illegible]										

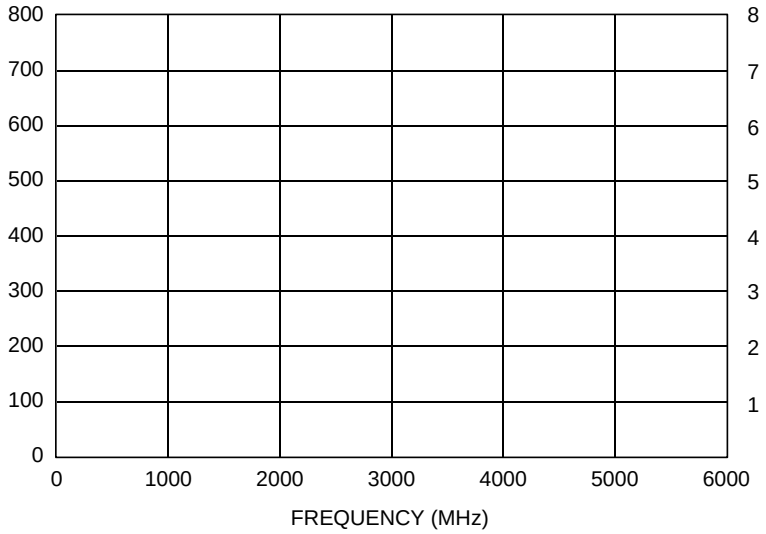


Figure 3. Frequency vs. V_{OUTpp} and JITTER

Resource Reference of Application Notes

AN1405/D − ECL Clock Distribution Techniques

AN1406/D − Designing with PECL (ECL at +5.0 V)

AN1503/D − ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D − Metastability and the ECLinPS Family

AN1568/D − Interfacing Between LVDS and ECL

AN1672/D − The ECL Translator Guide

AND8001/D − Odd Number Counters Design

AND8002/D − Marking and Date Codes

AND8020/D − Termination of ECL Logic Devices

AND8066/D − Interfacing with ECLinPS

AND8090/D − AC Characteristics of ECL Devices

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