

D[0:3]*, $\overline{D}$ [0:3]*	ECL Differential Data Inputs
Q[0:3], $\overline{Q}$ [0:3]	ECL Differential Data Outputs
V <sub>BB</sub>	Reference Voltage Output
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply

\* Pins will default LOW when left open.

$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		6	V
----------	------------------------	-----------------------	--	---	---





(V<sub>CC</sub> = 3.3 V, V<sub>EE</sub> = 0 V (Note 1))

		-									
I <sub>EE</sub>	Power Supply Current	47	55	63	50	58	66	54	62	70	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V <sub>BB</sub>	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	2.0		3.3	2.0		3.3	2.0		3.3	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.3 V to -2.2 V.
2. All loading with 50 Ω to V<sub>CC</sub> - 2.0 V.
3. V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>. V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal.

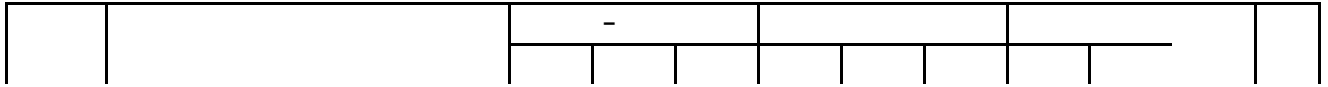
(V<sub>CC</sub> = 5.0 V, V<sub>EE</sub> = 0 V (Note 1))

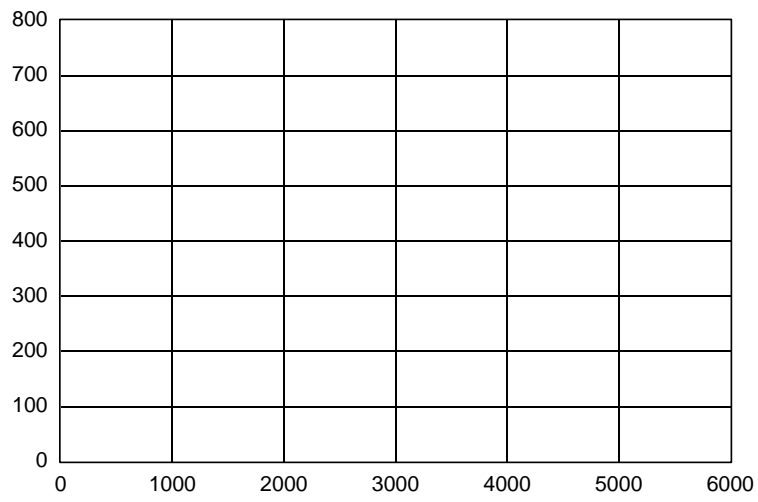
		-									
I <sub>EE</sub>	Power Supply Current	47	55	63	50	58	66	54	62	70	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
V <sub>IH</sub>	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
V <sub>IL</sub>	Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
V <sub>BB</sub>	Output Voltage Reference	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	2.0		5.0	2.0		5.0	2.0		5.0	V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +2.0 V to -0.5 V.
2. All loading with 50 Ω to V<sub>CC</sub> - 2.0 V.
3. V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>. V<sub>IHCMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal.

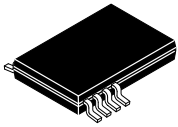
( $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 1))





- ECL Clock Distribution Techniques
- Designing with PECL (ECL at +5.0 V)
- ECLinPS™ I/O SPiCE Modeling Kit
- Metastability and the ECLinPS Family
- Interfacing Between LVDS and ECL
- The ECL Translator Guide
- Odd Number Counters Design
- Marking and Date Codes
- Termination of ECL Logic Devices
- Interfacing with ECLinPS
- AC Characteristics of ECL Devices





SCALE 2:1

**TSSOP-20 WB**  
CASE 948E  
ISSUE D

DATE 17 FEB 2016

**onsemi**, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**

---

---