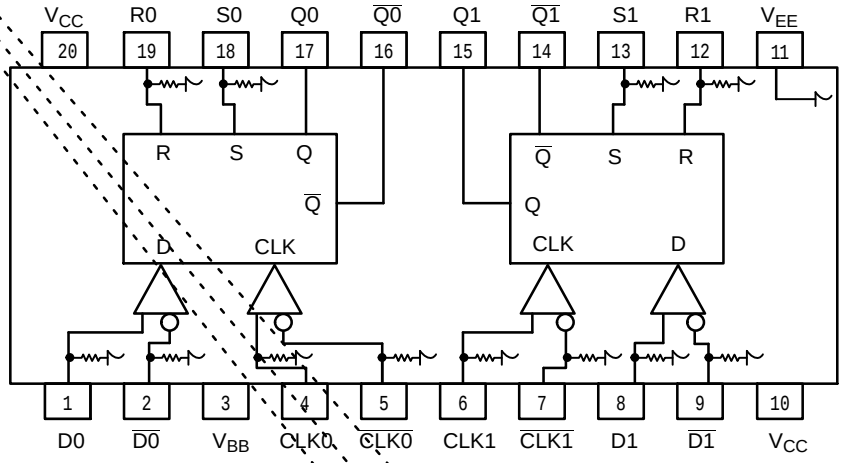

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.6789

Figure 1. 20−Lead Pinout (Top View) **and Logic Diagram**

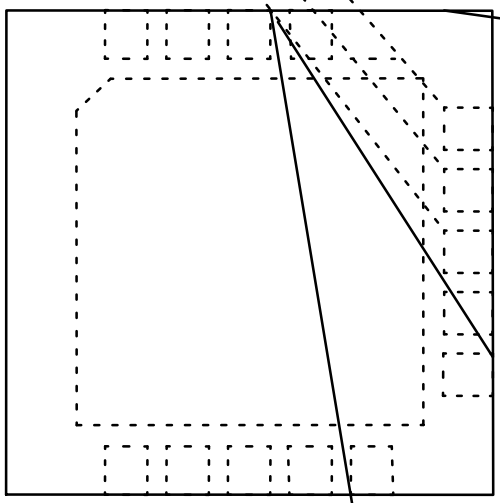

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	 > 2 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb−Free Pkg
TSSOP−20 QFN−20	Level 3 Level 1
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V−0 @ 0.125 in
Transistor Count	383 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			0.5	mA
T_A	Operating Temperature Range			−40 to +85	C
T_{stg}	Storage Temperature Range			−65 to +150	C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	20 TSSOP 20 TSSOP	140 100	C/W C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	20 TSSOP	23 to 41	C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	QFN−20 QFN−20	47 33	C/W C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	QFN−20	18	C/W
T_{sol}	Wave Solder (Pb−Free)			265	C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. 10EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 2)

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	35	46	55	37	48	57	40	49	60	mA
V_{OH}	Output HIGH Voltage (Note 3)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 3)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage (Single−Ended)	1365		1690	1460		1755	1490		1815	mV

Table 7. 10EP DC CHARACTERISTICS, NECL V_{CC} = 0 V; V_{EE} = −5.5 V to −3.0 V (Note 8)

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	35	46	55	37	48	57	40	49	60	mA
VOH	Output HIGH Voltage (Note 9)	−1135	−1010	−885	−1070	−945	−820	−1010	−885	−760	mV
V_{OL}	Output LOW Voltage (Note 9)	−1935	−1810	−1685	−1870	−1745	−1620	−1810	−1685	−1560	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	−1210		−885	−1145		−820	−1085		−760	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1935		−1610	−1870		−1545	−1810		−1485	mV
V_{BB}	Output Voltage Reference	−1510	−1410	−1310	−1445	−1345	−1245	−1385	−1285	−1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10)	V_{EE} + 2.0		0.0	V		0.0	V		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5									

Table 9. 100EP DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 14)

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}											

Table 11. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.0 V to −5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 20)

Symbol	Characteristic	−40 C			25 C			85 C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 2 F_{max}/JITTER)		> 3.0			> 3.0			> 3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay to CLK Output Differential S R	300 275 300	380 380 400	450 475 500	350 300 325	420 400 420	500 500 525	400 350 375	470 450 470	550 550 575	ps
t_S t_H	Setup Time Hold Time	100 100	20 20		100 100	20 20		100 100	20 20		ps
t_{RR}/t_{RR2}	Set/Reset Recovery	150	80		150	80		150	80		ps
t_{PW}	Minimum Pulse Width Set, Reset	500	300		500	300		500	300		ps
t_{JITTER}	Cycle−to−Cycle Jitter (See Figure 2 F_{max}/JITTER)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Note 21)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% − 80%)	100	180	250	150	210	300	175	230	325	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

20. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} − 2.0 V.

21. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

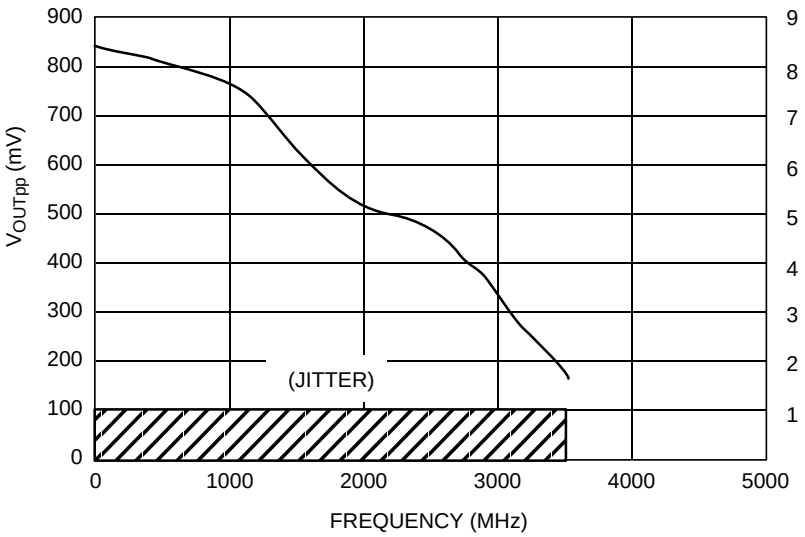

Figure 2. F_{max}/Jitter

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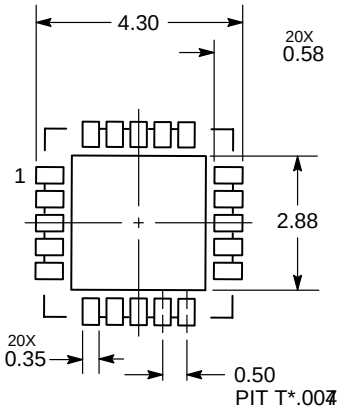

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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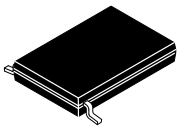
*For additional information on our Pb−Free strategy and soldering details, please download the Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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