3.3 V/5 V ECL ÷4 Divider

MC10EP33, MC100EP33

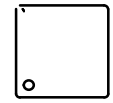
Description

The MC10/100EP33 is an integrated ÷4 divider. The differential clock inputs.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The reset pin is asynchronous and is asserted on the rising edge. Upon powerup, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple EP33's in a system.

The 100 Series contains temperature compensation.



Features

- 320 ps Propagation Delay
- Maximum Frequency = > 4 GHz Typical
- PECL Mode Operating Range:
  V_{CC} = 3.0 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range:
  V_{CC} = 0 V with V_{EE} = ĭ3.0 V to ĭ5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- V_{BB} Output
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

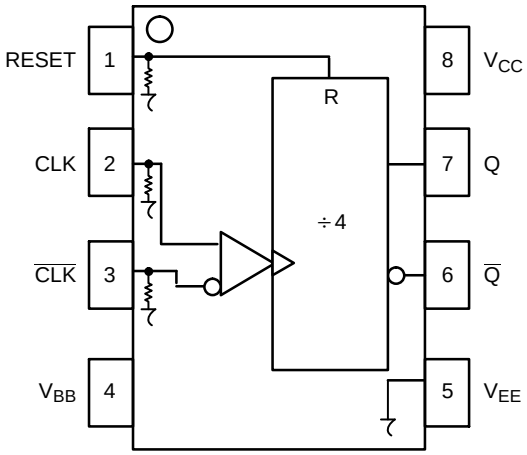


Figure 1. 8-Lead Pinout (Top View) **and Logic Diagram**

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK*, $\overline{CLK}$*	ECL Clock Inputs
Reset*	ECL Asynchronous Reset
V_{BB}	Reference Voltage Output
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

* Pins will default LOW when left open.

Table 2. TRUTH TABLE

CLK	$\overline{CLK}$	RESET	Q	$\overline{Q}$
X	X	Z	L	H
Z	$\overline{Z}$	L	F	F

Z = LOW to HIGH Transition
$\overline{Z}$ = HIGH to LOW Transition
F = Divide by 4 Function

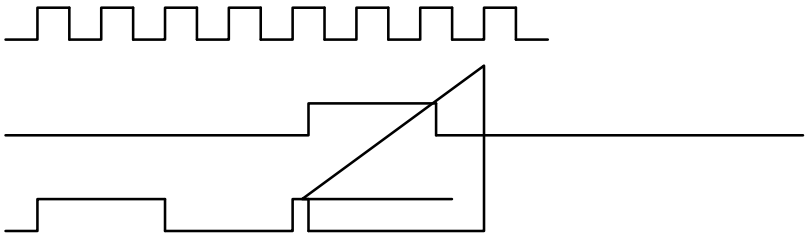


Figure 2. Timing Diagram

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V			

Table 6. 10EP DC CHARACTERISTICS, PECL (V_{CC} = 5.0 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	18	26	40	18	26	40	18	26	40	mA
V_{OH}	Output HIGH Voltage (Note 2)	3865	3990	4115	3930	4055	4180	3990			

Table 8. 100EP DC CHARACTERISTICS, PECL (V_{CC} = 3.3 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic

Table 10. 100EP DC CHARACTERISTICS, NECL (V_{CC} = 0 V; V_{EE} = −5.5 V to −3.0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	18	26	40	23	26	45	23	26	45	mA
V_{OH}	Output HIGH Voltage (Note 2)	−1145	−1020	−895	−1145	−1020	−895	−1145	−1020	−895	mV
V_{OL}	Output LOW Voltage (Note 2)	−1945	−1820	−1695	−1945	−1820	−1695	−1945	−1820	−1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	−1225		−880	−1225		−880	−1225		−880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	−1945		−1625	−1945		−1625	−1945		−1625	mV
V_{BB}	Output Voltage Reference	−1525	−1425	−1325	−1525	−1425	−1325	−1525	−1425	−1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 3)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

ORDERING INFORMATION

Device	Package	Shipping†
MC100EP33DG	SOIC−8 NB (Pb-Free)	98 Units / Tube
MC100EP33DTG	TSSOP−8 (Pb-Free)	100 Units / Tube
MC10EP33DR2G	SOIC−8 NB (Pb-Free)	2500 / Tape & Reel
MC100EP33DTR2G	TSSOP−8 (Pb-Free)	2500 / Tape & Reel
MC100EP33MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

DISCONTINUED (Note 2)

Device	Package	Shipping†
MC10EP33DG	SOIC−8 NB (Pb-Free)	98 Units / Tube
MC10EP33DTG	TSSOP−8 (Pb-Free)	100 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

2. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

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CASE 506AA
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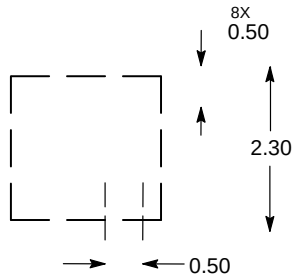
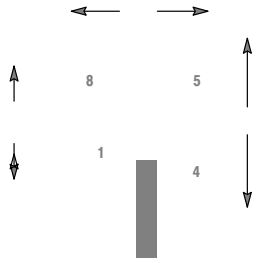


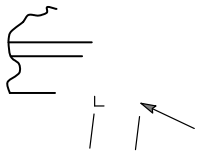
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the m1 □ Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOIC 8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011





SEATING
PLANE

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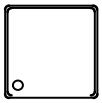
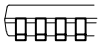
CASE 948R−02
ISSUE A

DATE 07 APR 2000





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B				
