

D [0:5]*, $\bar{D}$	

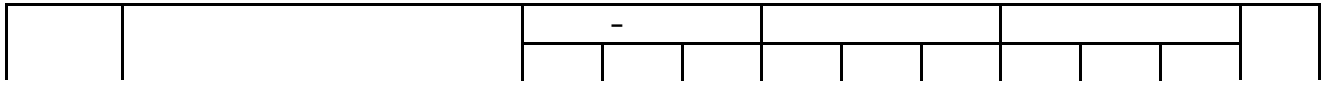
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Internal Input Pulldown Resistor	75 k $\Omega$
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 2 kV > 200 V > 2 kV





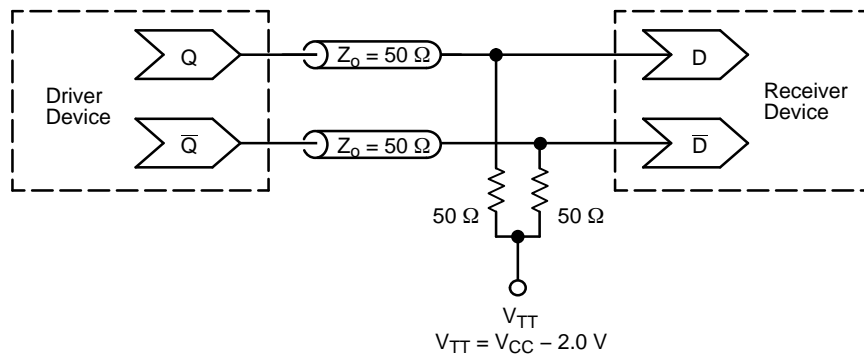
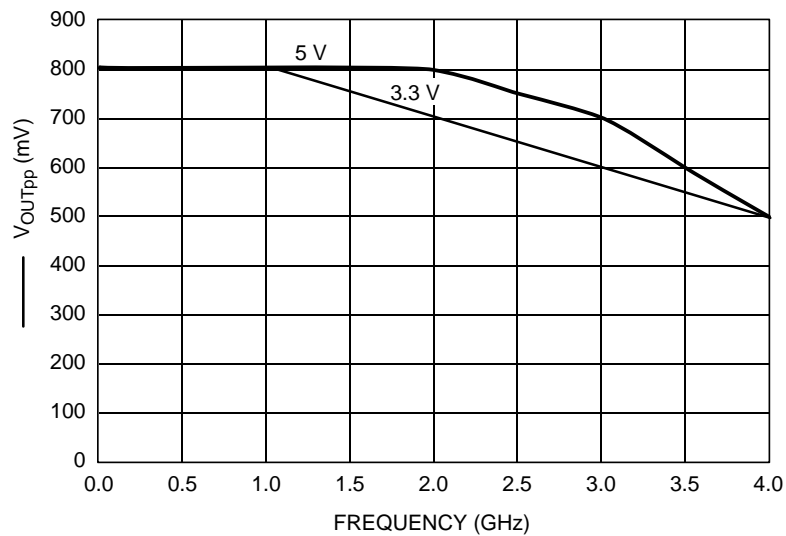
$V_{CC} = 3.3 \text{ V}$ ,  $V_{EE} = 0 \text{ V}$  (Note 7)



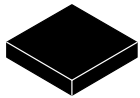
$I_{EE}$







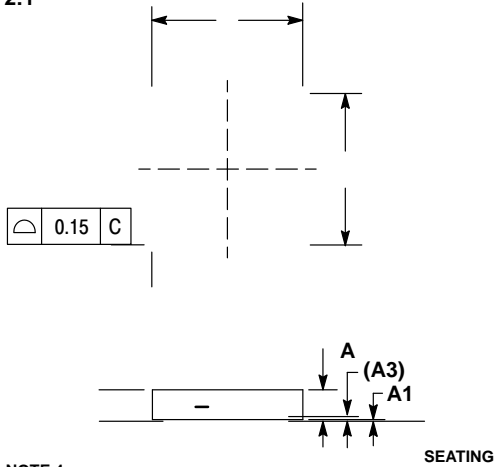
- ECL Clock Distribution Techniques
- Designing with PECL (ECL at +5.0 V)
- ECLinPS™ I/O SPICE Modeling Kit
- Metastability and the ECLinPS Family
- Interfacing Between LVDS and ECL
- The ECL Translator Guide
- Odd Number Counters Design
- Marking and Date Codes
- Termination of ECL Logic Devices
- Interfacing with ECLinPS
- AC Characteristics of ECL Devices



**QFN32 5x5, 0.5P**  
CASE 488AM  
ISSUE A

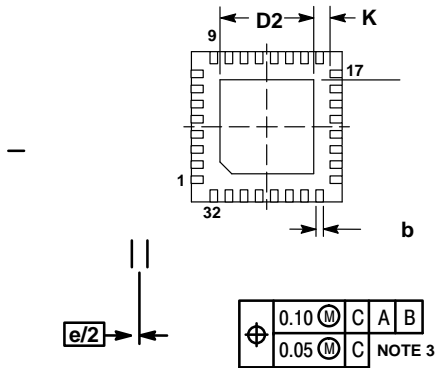
DATE 23 OCT 2013

SCALE 2:1

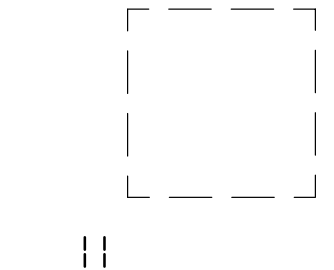


NOTE 4

	MAX
A1	0.80 1.00
A3	0.20 REF 0.05
b	0.18 0.30
D	5.00 BSC
D2	2.95 3.25
E	5.00 BSC
E2	2.95 3.25
e	0.50 BSC
K	0.20
L	0.30 0.50
L1	0.15



RECOMMENDED



PITCH

DIMENSION: MILLIMETERS

XXXXXXXXXX  
XXXXXXXXXX  
AWLYYYWW■  
■Free indicator, "G" or

DOCUMENT NUMBER:	98AON20032D	



**LQFP-32, 7x7**  
CASE 561AB  
ISSUE O

DATE 19 JUN 200

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