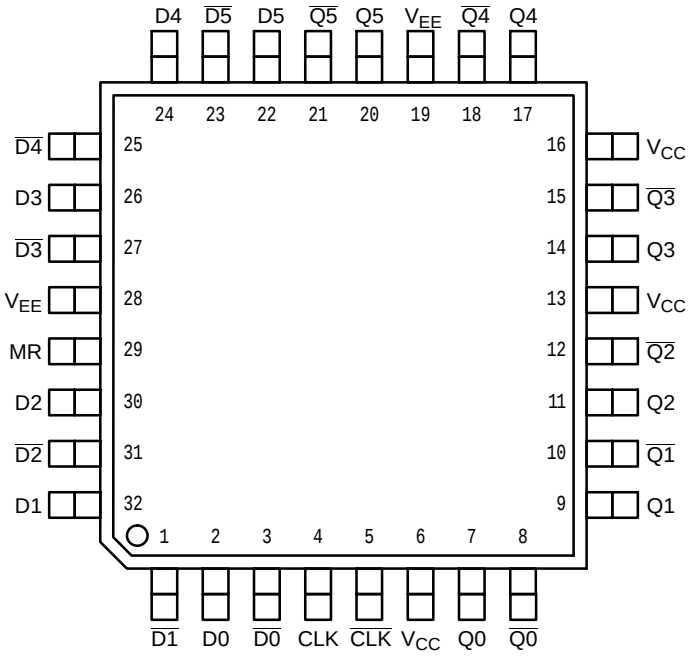
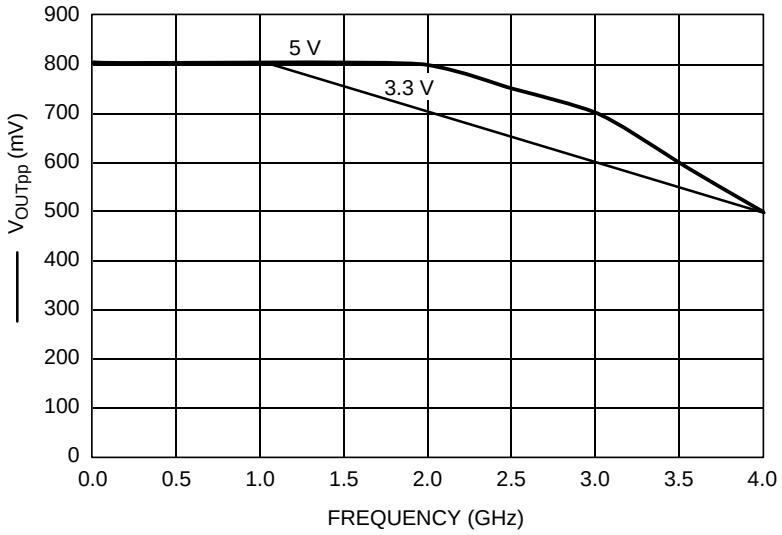

D4
D5
D5
Q5
Q5
VEE
Q4
Q4
24
23
22
21
20
19
18
17
D4
25
16
VCC
D3
26
15
Q3
D3
27
14
Q3
VEE
28
13
VCC
MR
29
12
Q2
D2
30
11
Q2
D2
31
10
Q1
D1
32
9
Q1
1
2
3
4
5
6
7
8
D1
D0
D0
CLK
CLK
VCC
Q0
Q0

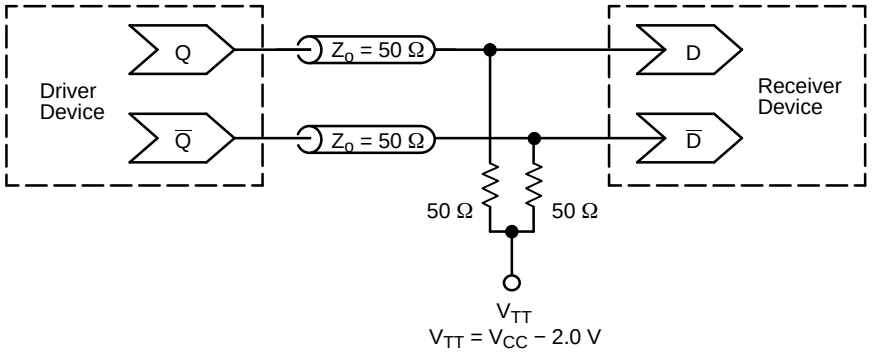
D [0:5]*, D	

Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 2 kV > 200 V > 2 kV

V_{CC} = 3.3 V, V_{EE} = 0 V (Note 7)

		–									
I_{EE}											





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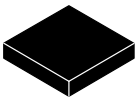
- ECL Clock Distribution Techniques
- Designing with PECL (ECL at +5.0 V)
- ECLinPS™ I/O SPiCE Modeling Kit
- Metastability and the ECLinPS Family
- Interfacing Between LVDS and ECL
- The ECL Translator Guide
- Odd Number Counters Design
- Marking and Date Codes
- Termination of ECL Logic Devices
- Interfacing with ECLinPS
- AC Characteristics of ECL Devices

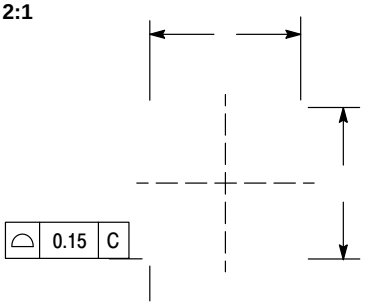
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

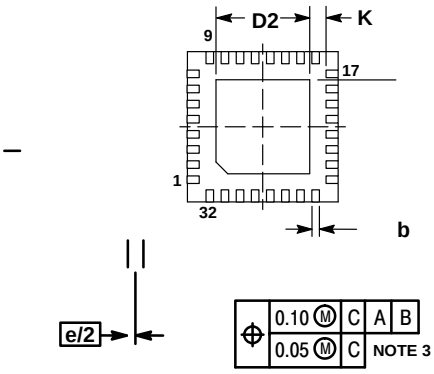
DATE 23 OCT 2013



SCALE 2:1

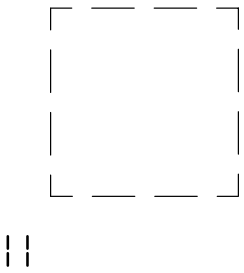


	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



XXXXXXXX
XXXXXXXX
AWLYYWW▪
▪Free indicator, “G” or

RECOMMENDED



PITCH

DIMENSION: MILLIMETERS

DOCUMENT NUMBER:	98AON20032D	

LQFP−32, 7x7
CASE 561AB
ISSUE O

DATE 19 JUN 200