3.3 V/5 V ECL D Flip-Flop with Reset and Differential Clock

MC10EP51, MC100EP51

SOIC−8
D SUFFIX
CASE 751

TSSOP−8
DT SUFFIX
CASE 948R

MARKING DIAGRAM

HP51
ALYW▪
▪

KP51
ALYW▪
▪

H = MC10
K = MC100
5S = MC10
$\overline{M}$ = Date Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

Description

The MC10/100EP51 is a differential clock D flip−flop with reset. The device is functionally equivalent to the EL51 and LVEL51 devices.

The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip−flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EP51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input conditions. When left open, the CLK input will be pulled down to V_{EE} and the $\overline{CLK}$ input will be biased at $V_{CC}/2$.

The 100 Series contains temperature compensation.

Features

- 350 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range: V_{CC} = 3.0 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −3.0 V to −5.5 V
- Open Input Default State
- Safety Clamp on Inputs
- These Devices are Pb−Free and are RoHS Compliant

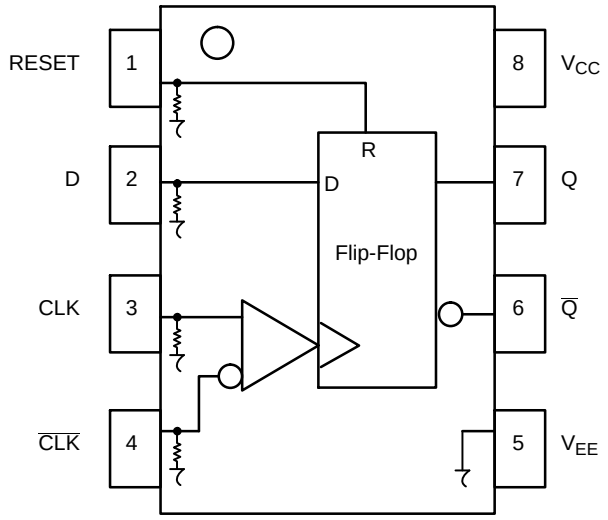


Figure 1. 8−Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK*, $\overline{CLK}$*	ECL Clock Inputs
Reset*	ECL Asynchronous Reset
D*	ECL Data Input
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

* Pins will default LOW when left open.

Table 2. TRUTH TABLE

D	R	CLK	Q
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 2 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb−Free Pkg
SOIC−8 TSSOP−8 DFN8	Level 1 Level 3 Level 1
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V−0 @ 0.125 in
Transistor Count	165 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 10. 100EP DC CHARACTERISTICS, NECL V_{CC} = 0 V; V_{EE} = −5.5 V to −3.0 V (Note 18)

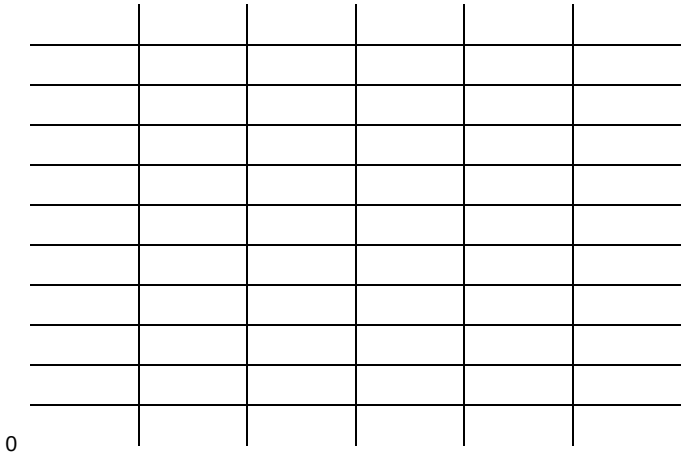
Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	26	34	44	26	35	45	28	37	47	mA
V_{OH}	Output HIGH Voltage (Note 19)	−1145	−1020	−895	−1145	−1020	−895	−1145	−1020	−895	mV
V_{OL}	Output LOW Voltage (Note 19)	−1945	−1820	−1695	−1945	−1820	−1695	−1945	−1820	−1695	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	−1225		−880	−1225		−880	−1225		−880	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1945		−1625	−1945		−1625	−1945		−1625	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 20)	V_{EE} + 2.0		0.0	V_{EE} + 2.0		0.0	V_{EE} + 2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

18. Input and output parameters vary 1:1 with V_{CC}.
19. All loading with 50 Ω to V_{CC} − 2.0 V.
20. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 11. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.0 V to −5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 21)

Symbol	Characteristic		−40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (Figure 2)			> 3			> 3			> 3		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential CLK, $\overline{CLK}$ to Q, $\overline{Q}$	10	250	300	350	270	320	370	300	350	420	ps
		100	275	340	425	300	375	450	350	425	500	
	RESET to Q, $\overline{Q}$		300	380	450	325	400	475	350	425	500	
t_{RR}	Reset Recovery		150			150			150			ps



ORDERING INFORMATION

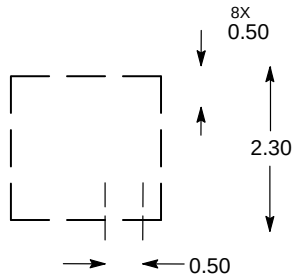
Device	Package	Shipping†
MC10EP51DR2G	SOIC−8 (Pb−Free)	

DF 8 2□2, 0.5
CASE 506AA
ISSUE F

DATE 04 MAY 2016

1
CA E 4:1

DE I G F I *

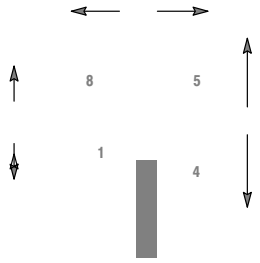


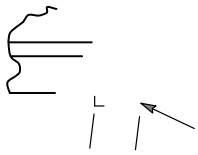
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the m1 □ Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOIC 8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

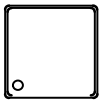


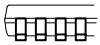


SEATING
PLANE

TSSOP 8 3.00x3.00x0.95
CASE 948R−02
ISSUE A

DATE 07 APR 2000





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B				
