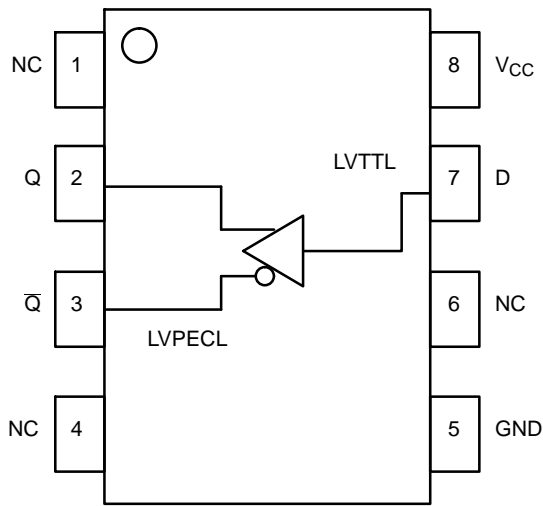


**3.3 V LVTTL/LVCMOS to
Differential LVPECL
Translator**

MC10EPT20, MC100EPT20



Q, \bar{Q}	Differential PECL Outputs
D	LVTTL Input
V _{CC}	Positive Supply
GND	Ground
NC	No Connect

-

V_{CC}	Power Supply	GND = 0 V		6	V
V_I	Input Voltage	GND = 0 V	V_I V_{CC}	6	V
I_{out}	Output Current	Continuous Surge		50 100	mA



(V_{CC} = 3.3 V, GND = 0 V (Note 1))

		-									
I _{CC}	Positive Power Supply Current	20	25	30	22	27	32	23	28	33	mA
V _{OH}	Output HIGH Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V _{OL}	Output LOW Voltage (Note 2)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

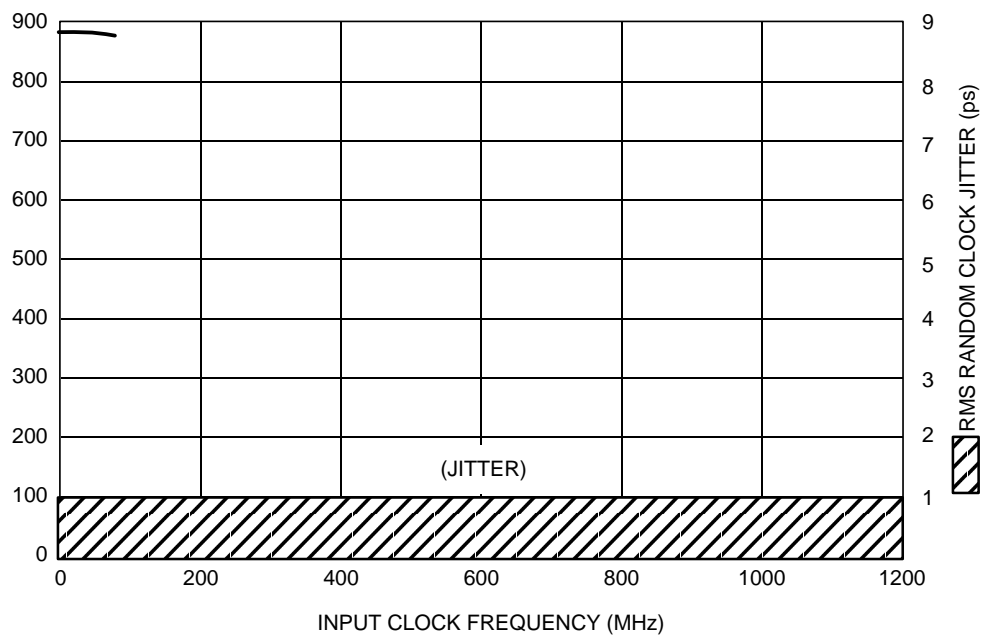
1. Output parameters vary 1:1 with V_{CC}.
2. All loading with 50 Ω to V_{CC} 2.0 V.

(V_{CC} = 3.0 V to 3.6 V, GND = 0 V (Note 1))

		-									
f _{max}	Maximum Input Clock Frequency		> 1			> 1			> 1		GHz
t _{PLH} , t _{PHL}	Propagation Delay to Output Differential	280	350	430	300	370	450	320	400	490	ps
t _{SKEW}	Device-to-Device Skew (Note 2)			150			150			170	ps
t _{JITTER}	RMS Random Clock Jitter		1	2		1	2		1	2	ps
t _r t _f	Output Rise/Fall Times Q, \bar{Q} (20% 80%)	70	100	170	80	120	180	90	140	190	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

1. Measured using a LVTTTL source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} 2.0 V.
2. Skew is measured between outputs under identical transitions.



		†
MC10EPT20DG	SOIC 8 NB (Pb-Free)	98 Units/Tube
MC100EPT20DG	SOIC 8 NB (Pb-Free)	98 Units/Tube
MC100EPT20DR2G	SOIC 8 NB (Pb-Free)	2500 / Tape & Reel
MC100EPT20DTG	TSSOP 8 (Pb-Free)	100 Units/Tube
MC100EPT20DTR2G	TSSOP 8 (Pb-Free)	2500 / Tape & Reel
MC100EPT20MNR4G	DFN 8 (Pb-Free)	1000 / Tape & Reel

(Note 3)

MC10EPT20DTG	TSSOP 8 (Pb-Free)	100 Units/Tube
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†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

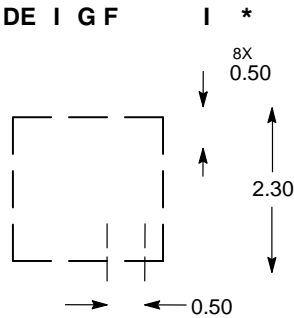
3. This device is not recommended for new design. Please contact your representative for information. The most current information on this device may be available on www.onsemi.com.

ECL Clock Distribution Techniques
 Designing with PECL (ECL at +5.0 V)
 ECLinPS™ I/O SPiCE Modeling Kit
 Metastability and the ECLinPS Family
 Interfacing Between LVDS and ECL
 The ECL Translator Guide
 Odd Number Counters Design
 Marking and Date Codes
 Termination of ECL Logic Devices
 Interfacing with ECLinPS
 AC Characteristics of ECL Devices

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CASE 506AA
ISSUE F

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DATE 04 MAY 2016

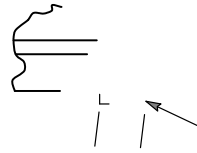
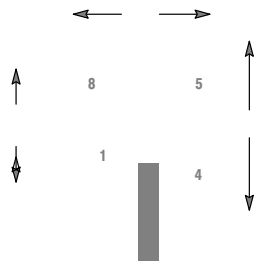


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the [m\] □ Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.](#)

SOIC 8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



SEATING
PLANE



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