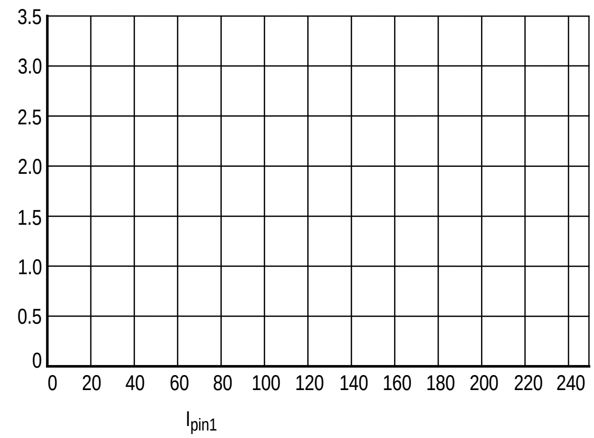
ELECTRICAL CHARACTERISTICS (V_{CC} = 13 V, T_J = 25 C for typical values, T_J = −40 to 105 C for min/max values unless otherwise noted.)

Characteristic	Pin # PDIP-8	Pin # SO-8	Symbol	Min	Typ	Max	Unit
REGULATION SECTION (continued)							
Feedback Pin Clamp Voltage @ I_{FB} = 100 mA	1	7	V_{FB-100}	1.5	2.1	2.5	V
Feedback Pin Clamp Voltage @ I_{FB} = 200 mA	1	7	V_{FB-200}	2.0	2.6	3.0	V
CURRENT SENSE SECTION							
Zero Current Detection Comparator Threshold	4	2	V_{ZCD-th}	−90	−60	−30	mV
Negative Clamp Level (I_{CS-pin} = −1.0 mA)	4	2	Cl−neg	−	−0.7	−	V
Bias Current @ Vcs = V_{ZCD-th}	4	2	I_{b-cs}	−0.2	−	−	mA

Pin Numbers are Relevant to the PDIP-8 Version



JUNCTION TEMPERATURE (C)

Pin Numbers are Relevant to the PDIP-8 Version

104

OSCILLATOR CHARGE CURRENT (A)

−40

Figure 9. Oscillator Charge Current versus Temperature

120

ON-TIME (s)

30

Figure 10. On-Time versus Feedback Current

75

50

Figure 11. On-Time versus Feedback Current

207

−40

Figure 12. Internal Current Sources versus Temperature

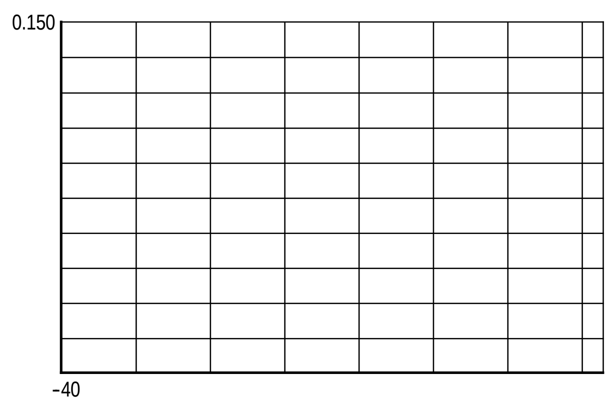


Figure 13. (I_{ovpH}/I_{ref}), (I_{ovpL}/I_{ref}), (I

Pin Numbers are Relevant to the PDIP‑8 Version

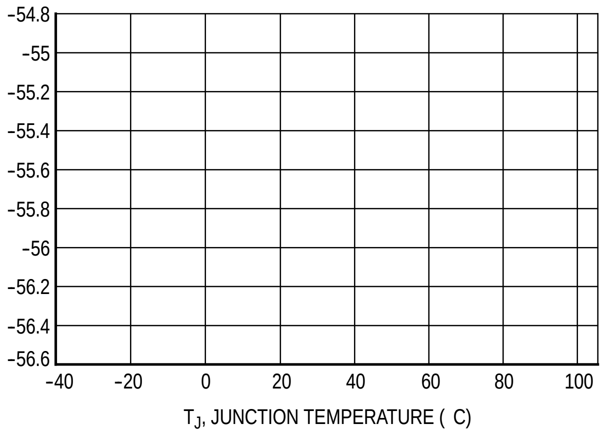


Figure 15. Current Sense Threshold versus Temperature

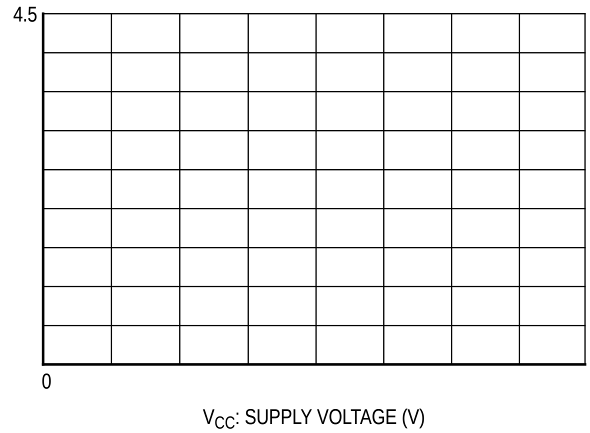


Figure 16. Circuit Consumption versus Supply Voltage

20

0

$V_{control}$: PIN 2 VOLTAGE (V)

Figure 17. Oscillator Pin Internal Capacitance

1

Ch1

Figure 18. Gate Drive Cross Conduction

Figure 19. Gate Drive Cross Conduction

Figure 20. Gate Drive Cross Conduction

PIN FUNCTION DESCRIPTION

Pin # PDIP-8	Pin # SO-8	Function	Description
1	7	Feedback Input	This pin is designed to receive a current that is proportional to the preconverter output voltage. This information is used for both the regulation and the overvoltage and undervoltage protections. The current drawn by this pin is internally squared to be used as oscillator capacitor charge current.
2	8	$V_{control}$	This pin makes available the regulation block output. The capacitor connected between this pin and ground, adjusts -276.7(c)415.5(squaC9.3(t)-1.3(he)-279.3(regulation)-279.3(b))-279.3(t)-579.3

FUNCTIONAL DESCRIPTION

Pin Numbers are Relevant to the PDIP-8 Version

INTRODUCTION

The need of meeting the requirements of legislation on

Pin Numbers are Relevant to the PDIP-8 Version

Consequently:

$$R_o = \frac{V_{o\ regH} - V_{pin1}}{I_{regH}}$$

In practice, V_{pin1} is small compared to $(V_o)_{regH}$ and this equation can be simplified as follows (I_{regH} being also replaced by its typical value 200 mA

$$R_o \approx 5 \times V_{o\ regH}\ (k\ \ )$$

The regulation block output is connected to the Pin 2 through a 300 k resistor. The Pin 2 voltage ($V_{control}$) is compared to the oscillator sawtooth for PWM control.

An external capacitor must be connected between Pin 2 and ground, for external loop compensation. The bandwidth is typically set below 20 Hz so that the regulation block output should be relatively constant over a given ac line cycle. This integration that results in a constant on-time over the ac line period, prevents the mains frequency output ripple from distorting the ac line current.

OSCILLATOR SECTION

The oscillator consists of three phases:

Charge Phase: The oscillator capacitor voltage grows up linearly from its bottom value (ground) until it exceeds $V_{control}$ (regulation block output voltage). At that moment, the PWM latch output gets low and the oscillator discharge sequence is set.

Discharge Phase: The oscillator capacitor is abruptly discharged down to its valley value (0 V).

Waiting Phase: At the end of the discharge sequence, the oscillator voltage is maintained in a low state until the PWM latch is set again.

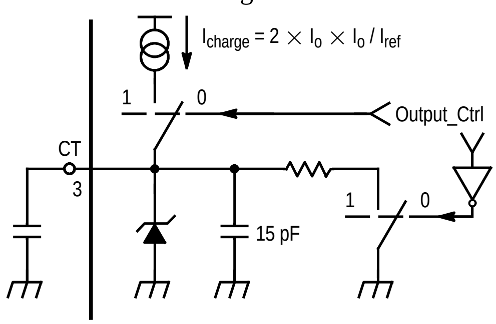


Figure 26. Oscillator

The oscillator charge current is dependent on the feedback current (I_o). In effect

$$I_{charge} = 2 \times \frac{I_o^2}{I_{ref}}$$

where:

I_{charge} is the oscillator charge current,

I_o

This equation shows that the maximum on-time is inversely proportional to the squared output voltage. This property is used for follower boost operation (refer to
section).

CURRENT SENSE BLOCK

The inductor current is converted into a voltage by inserting a ground referenced resistor (R_{cs}) in series with the input diodes bridge (and the input filtering capacitor). Therefore a negative voltage proportional to the inductor current is built:

$$V_{CS} = - R_{CS} \times I_L$$

where:

I_L is the inductor current,
R_{cs} is the current sense resistor,
V_{cs} is the measured R_{cs} voltage.

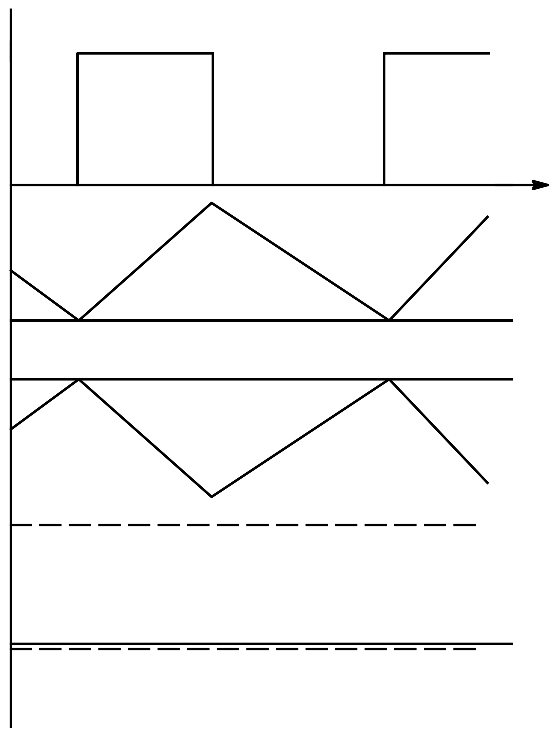


Figure 27. Current Sensing

Pin Numbers are Relevant to the PDIP-8 Version

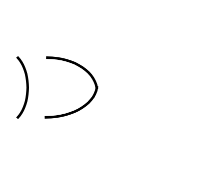


Figure 29. PWM Latch

Pin Numbers are Relevant to the PDIP-8 Version

In particular, a 11 V Zener diode is internally connected between the terminal and ground on the following pins: Feedback, $V_{control}$, Oscillator, Current Sense, and Synchronization.

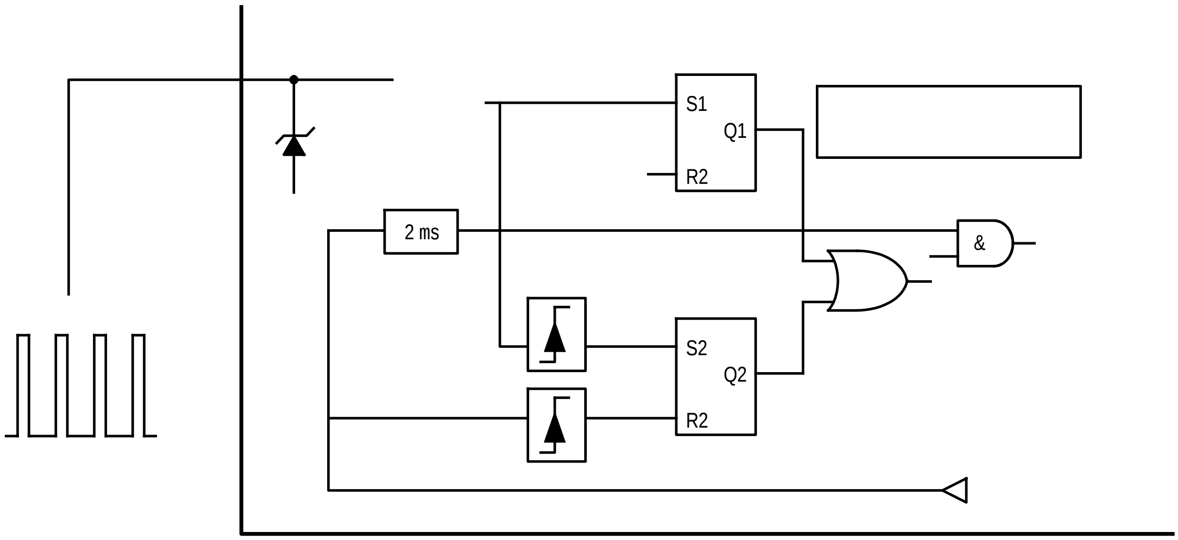


Figure 31. Synchronization Arrangement

Pin Numbers are Relevant to the PDIP-8 Version

FOLLOWER BOOST

Pin Numbers are Relevant to the PDIP-8 Version

On the other hand, the boost topology has its own rule that dictates the on-time necessary to deliver the required power:

$$t_{on} = \frac{4 \times L_p \times P_{in}}{V_{pk}^2}$$

where:

V_{pk} is the peak ac line voltage,
L_p is the inductor value,
P_{in} is the input power.

Combining the two equations, one can obtain the Follower Boost equation:

$$V_o = \frac{R_o}{2} \times \sqrt{\frac{C_{pin3}}{K_{osc} \times L_p \times P_{in}}} \times V_{pk}$$

Consequently, a linear dependency links the output voltage to the ac line amplitude at a given input power.

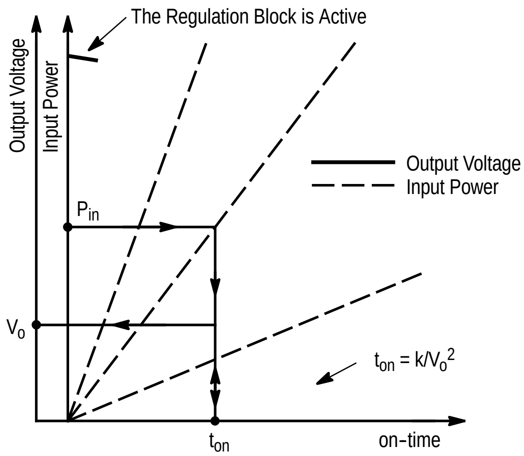


Figure 34. Follower Boost Characteristics

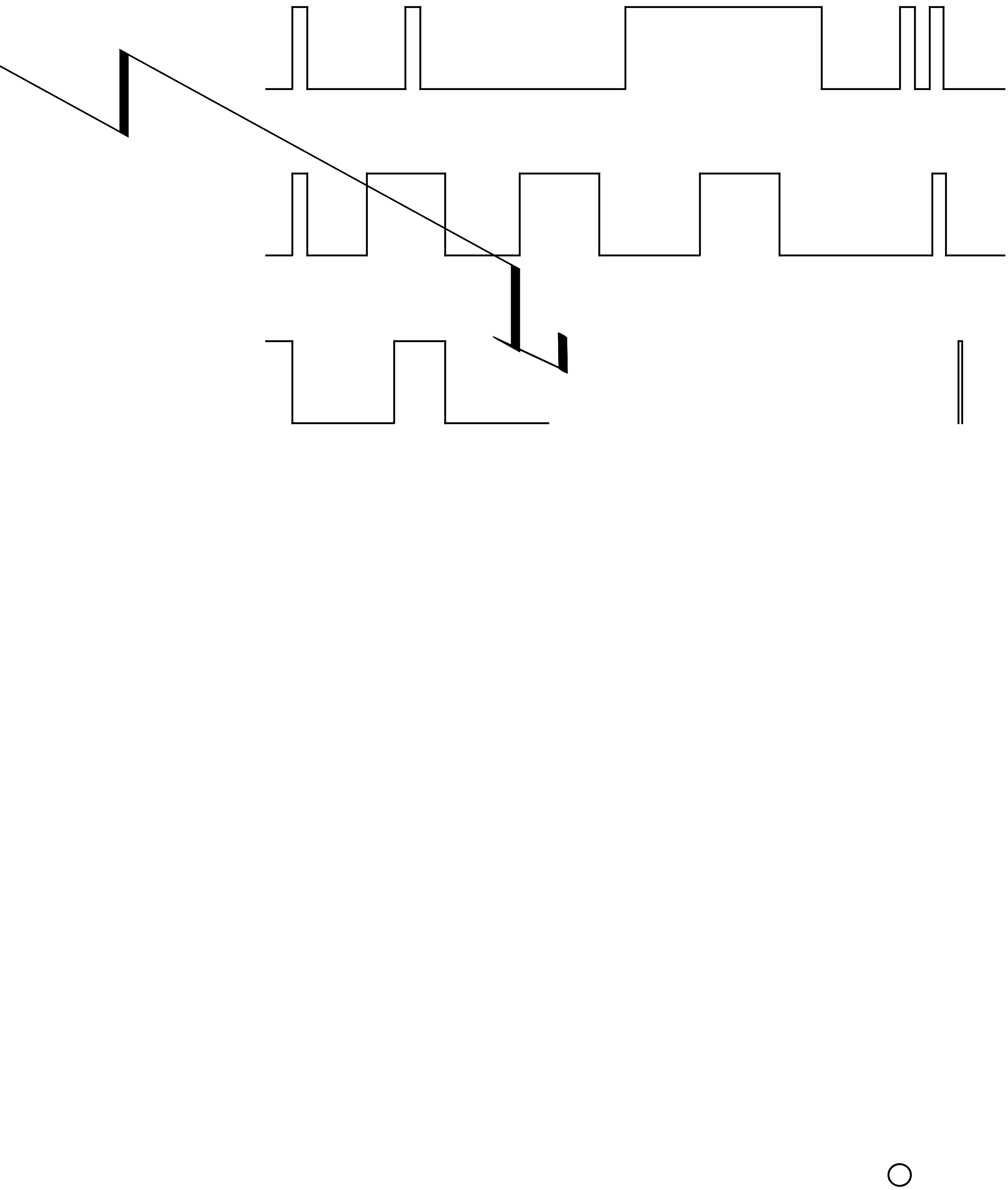


Figure 36. Typical Waveforms

MAIN DESIGN EQUATIONS (Note 3)

rms Input Current (I_{ac}) $I_{ac} = \frac{P_o}{\times V_{ac}}$	(preconverter efficiency) is generally in the range of 90 – 95%.
Maximum Inductor Peak Current ($(I_{pk})max$): $(I_{pk})\,max = \frac{2 \times \ \overline{2} \times (P_o)\,max}{\times V_{acLL}}$	$(I_{pk})max$ is the maximum inductor current.
Output Voltage Peak to Peak 100Hz (120Hz) Ripple ((Vo)pk–pk): $(\ V_o)_{pk-pk} = \frac{P_o}{2 \ \ \times f_{ac} \times C_o \times V_o}$	f_{ac} is the ac line frequency (50 or 60Hz).
Inductor Value (L_p): $L_p = \frac{2 \times t \times \ \frac{V_o}{\overline{2}} - V_{acLL} \ \times V_{acLL}{}^2}{V_o \times V_{acLL} \times (I_{pk})\,max}$	t is the maximum switching period. (t = 40 ms) for universal mains operation and (t = 20 ms) for narrow range are generally used.
Maximum Power MOSFET Conduction Losses ($(p_{on})max$): $(P_{on})\,max \approx \frac{1}{3} \times (Rds)on \times (I_{pk})\,max^2 \times \ \ 1 - \frac{1.2 \times V_{acLL}}{V_o}$	(Rds)on is the MOSFET drain source on–time resistor. In Follower Boost, the ratio (V_{acLL}/V_o) is higher. The on–time MOSFET losses are then reduced.
Maximum Average Diode Current (I_d): $(I_d)\,max = \frac{(P_o)\,max}{(V_o)\,min}$	The Average Diode Current depends on the power and on the output voltage.
Current Sense Resistor Losses (pR_{cs}): $pR_{cs} = \frac{1}{6} \times (Rds)on \times (I_{pk})^2\,max$	This formula indicates the required dissipation capability for R_{cs} (current sense resistor).
Over Current Protection Resistor (R_{OCP}): $R_{OCP} \approx \frac{R_{cs} \times (I_{pk})\,max}{0.205}$ (k)	The overcurrent threshold is adjusted by R_{OCP} at a given R_{cs}. R_{cs}

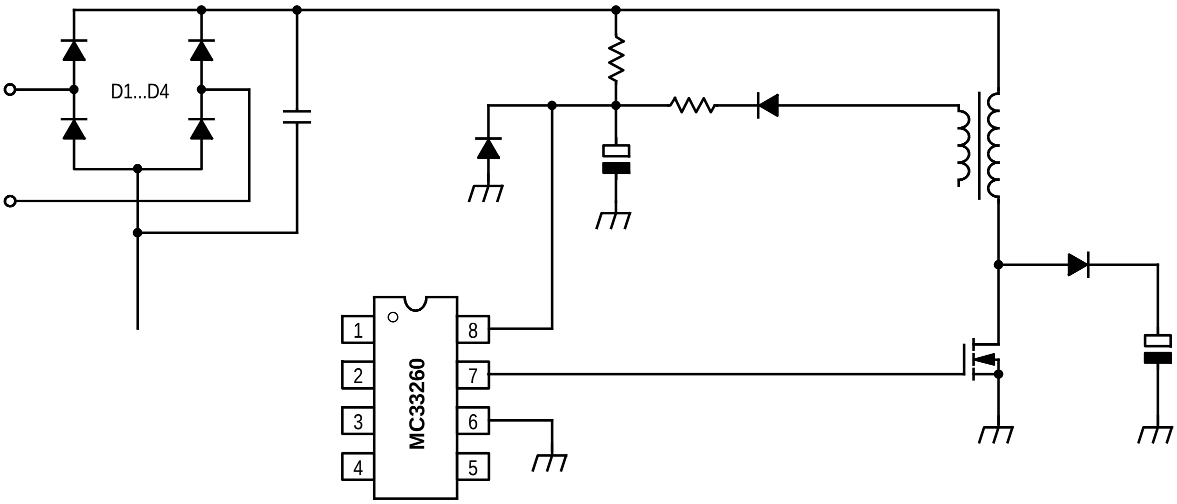


Figure 38. Circuit Supply Voltage

ORDERING INFORMATION

Device	Package	Shipping†
MC33260PG	PDIP−8 (Pb−Free)	50 Units / Rail
MC33260DG	SOIC−8 (Pb−Free)	98 Units / Rail
MC33260DR2G	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PDIP 8
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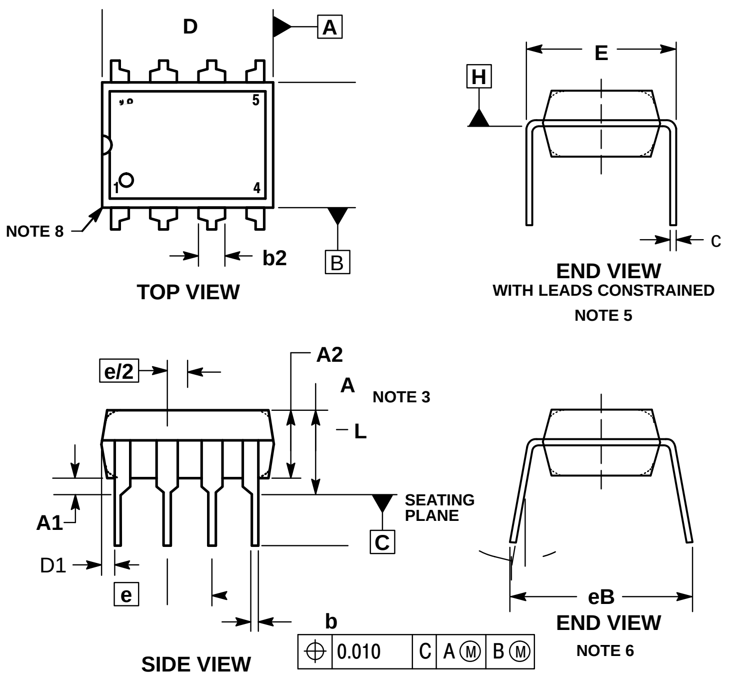
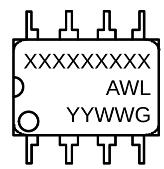
DATE 22 APR 2015



	INCHES			
DIM	MIN	MAX		
A	----	0.210		
A1	0.015	----		
A2	0.115	0.195	2.92	4.95
b	0.014	0.022		
C	0.008	0.014		
D	0.355	0.400		
D1	0.005	----		
E	0.300	0.325		
e	0.100 BSC			
L	0.115	0.150	2.92	3.81

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

SOIC 8 NB
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DATE 16 FEB 2011