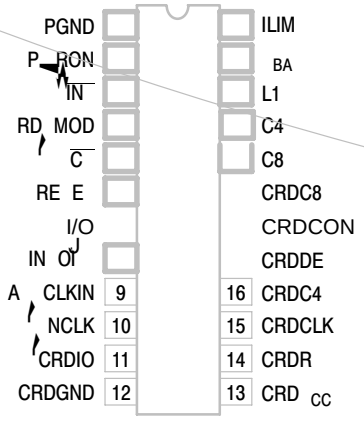
MC33560

Power Management and Interface IC for Smartcard Readers and Couplers

The MC33560 is an interface IC for smartcard reader/writer applications. It enables the management of any type of smart or memory card through a simple and flexible microcontroller interface. Moreover, several couplers can be coupled Tc0Wer

ON Semiconductor

http://onsemi.com



(Top View)

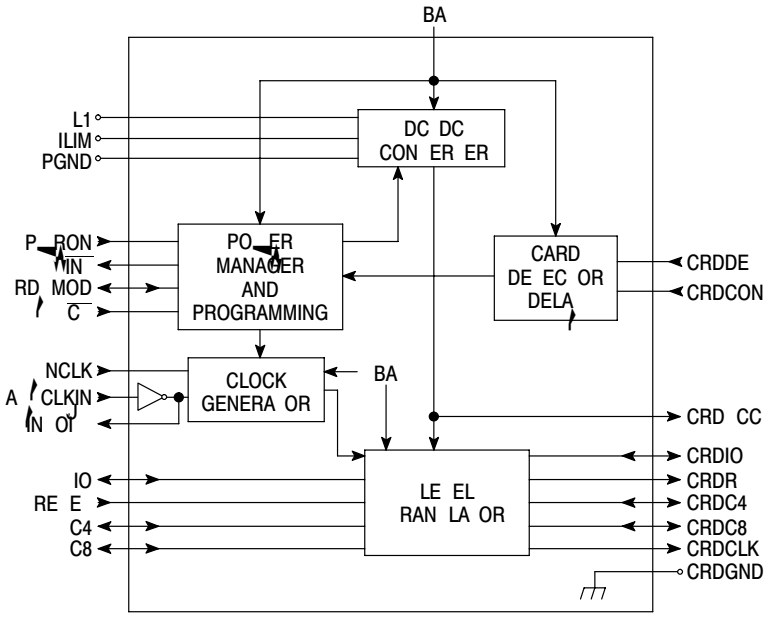


Figure 1. Simplified Functional Block Diagram

MAXIMUM RATINGS (Note 1)

Symbol	Rating	Value	Unit
V_{BAT}	Battery Supply Voltage	7.0	
BAT	Battery Supply Current	±200	

ELECTRICAL CHARACTERISTICS These specifications are written in the same style as common for standard integrated circuits. The convention considers current flowing into the pin (sink current) as positive and current flowing out of the pin (source current) as negative. (Conditions: V_{BAT} = 4.0 V, V_{CC} = 5.0 V nom, PWRON = V_{BAT} , Operating Mode, $-I_{CC}$ = 10 mA, $-25°C \le T_A \le 85°C$, L_1 = 47 μH, R_{LIM} = 0 Ω, CRDV_{CC} capacitor = 10 μF, unless otherwise noted.)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
BATTERY POWER SUPPLY SECTION						
Supply Voltage Range Normal operating range extended operating range (Note 4)		V_{BAT}	2.2 1.8	– –	6.0 6.6	V
MC33560 Standby Quiescent Current PWRON = GND, CRDCON = GND, ASYCLKIN = GND, V_{BAT} = 6.0 V, All Other Logic Inputs and Outputs Open		I_{oBAT}	–	–	30	μA
DC Operating Current $-I_{CC}$ = 10 mA; V_{CC} = 5.0 V, V_{BAT} = 6.0 V		I_{BATop}	–	–	12.5	mA

V_{BAT}

ELECTRICAL CHARACTERISTICS (continued) These specifications are written in the same style as common for standard integrated circuits. The convention considers current flowing into the pin (sink current) as positive and current flowing out of the pin (source current) as negative. (Conditions: V_{BAT} = 4.0 V, V_{CC} = 5.0 V nom, PWRON = V_{BAT} , Operating Mode, $-I_{CC}$ = 10 mA, $-25°C \le T_A \le 85°C$, L_1 = 47 μH, R_{LIM} = 0 Ω, CRDV_{CC} capacitor = 10 μF, unless otherwise noted.)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
APPLICATION INTERFACE DC SECTION (V_{BAT} = 5.0 V)						
Input High Threshold Voltage (increasing)	Pins 2, 4, 5, 6, 10, 17	V_{IH}	0.55*V_{BAT}	−	0.65*V_{BAT}	V
Input Low Threshold Voltage (decreasing)	Pins 2, 5, 6, 10 Pin 17 Pin 4	V_{IL}	0.3*V_{BAT} 0.2*V_{BAT} 0.3*V_{BAT}	− − −	0.45*V_{BAT} 0.40*V_{BAT} 0.5*V_{BAT}	V
Switching Hysteresis	Pins 2, 4, 5, 6, 10, 17	V				

ELECTRICAL CHARACTERISTICS (continued) These specifications are written in the same style as common for standard integrated circuits. The convention considers current flowing into the pin (sink current) as positive and current flowing out of the pin (source current) as negative. (Conditions: V_{BAT} = 4.0 V, V_{CC} = 5.0 V nom, PWRON = V_{BAT} , Operating Mode, $-I_{CC}$ = 10 mA, $-25°C \le T_A \le 85°C$, L_1 = 47 μH, R_{LIM} = 0 Ω, CRDV_{CC} capacitor = 10 μF, unless otherwise noted.)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit

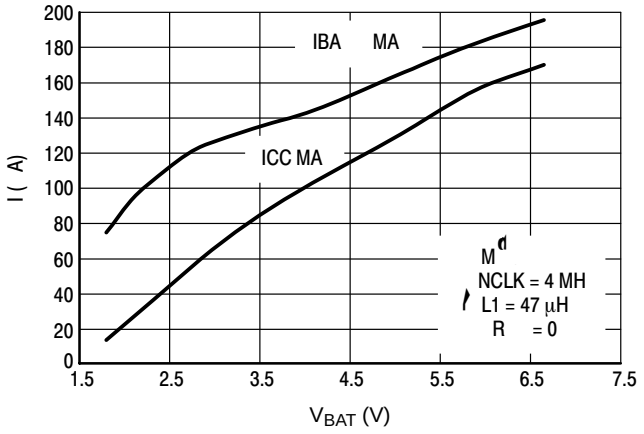


Figure 2. Maximum Battery and Card Supply Current vs. V_{BAT} (V_{CC} = 5.0 V)

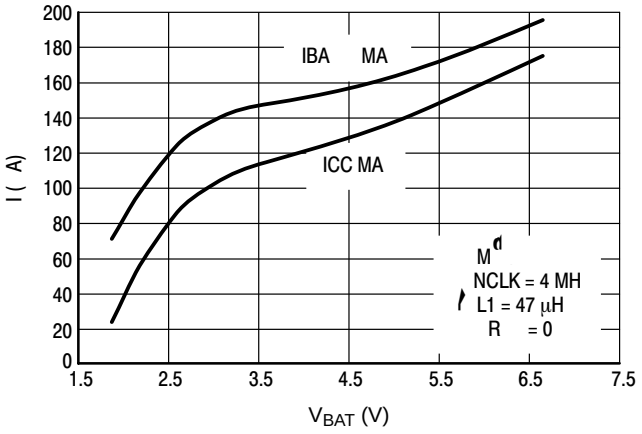


Figure 3. Maximum Battery and Card Supply Current vs. V_{BAT} (V_{CC} = 3.0 V)

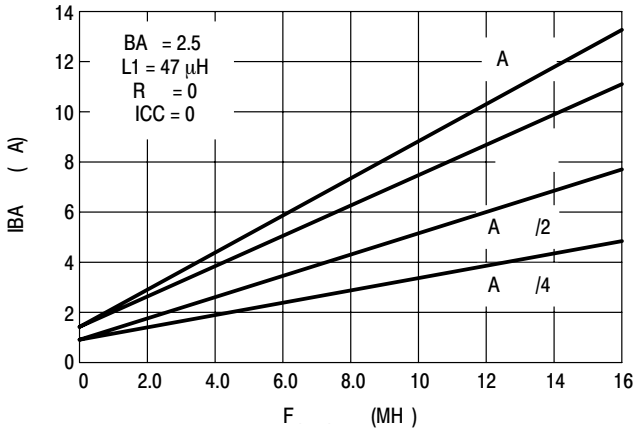


Figure 4. Battery Current vs. Input Clock Frequency (I_{CC} = 0, V_{BAT} = 4.0 V)

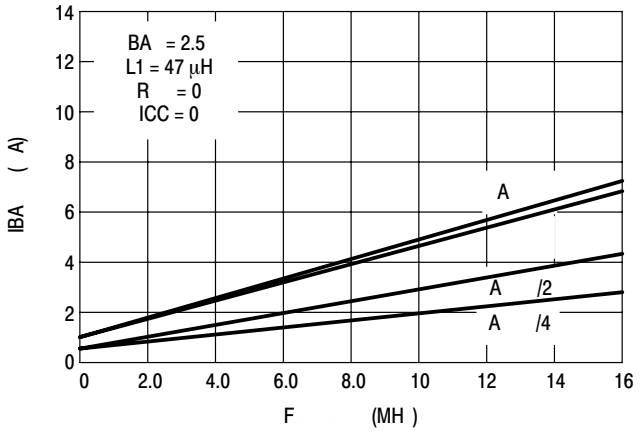


Figure 5. Battery Current vs. Input Clock Frequency (I_{CC} = 0, V_{BAT} = 2.5 V)

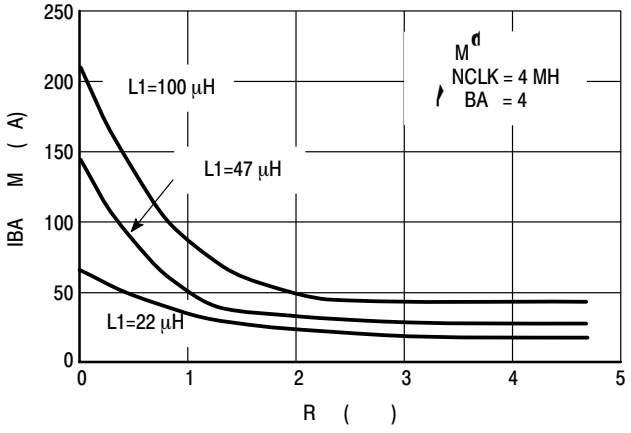


Figure 6. Maximum Battery Current vs. R_{LIM} (V_{CC} = 5.0 V, V_{BAT} = 4.0 V)

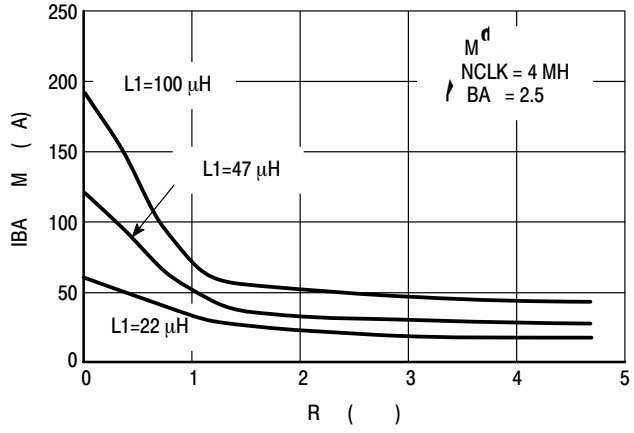
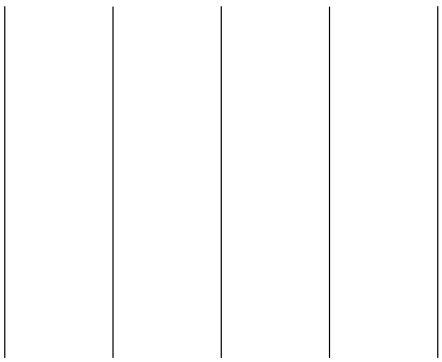


Figure 7. Maximum Battery Current vs. R_{LIM} (V_{CC} = 3.0 V, V_{BAT} = 2.5 V)



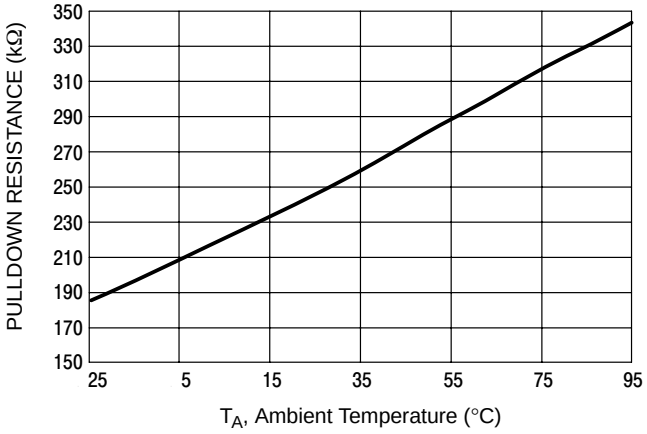


Figure 14. Pulldown Resistance vs. Temperature

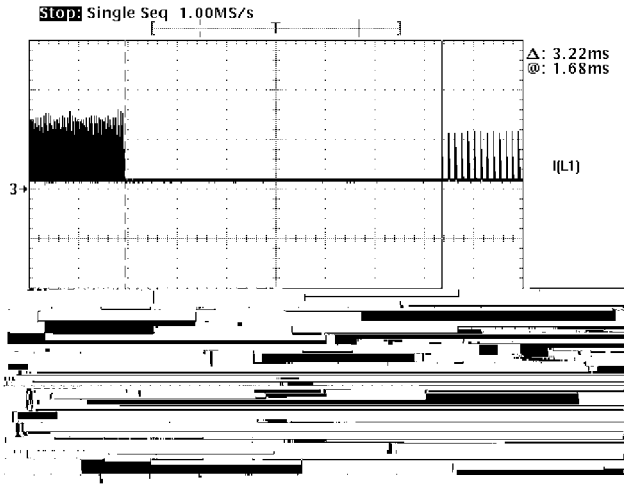


Figure 15. Transition from 5.0 V to 3.0 V Card Supply

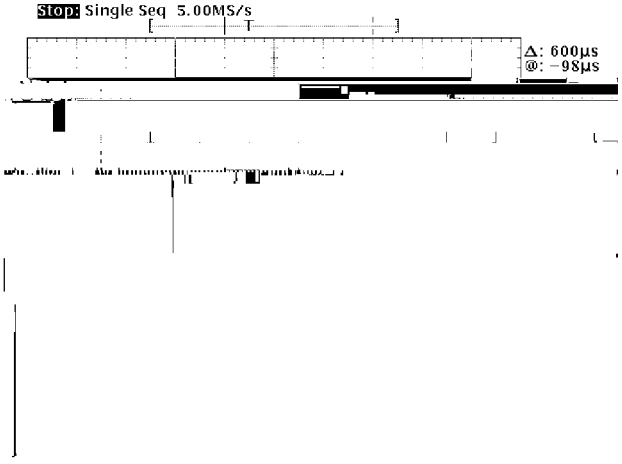


Figure 16. Transition from 3.0 V to 5.0 V Card Supply

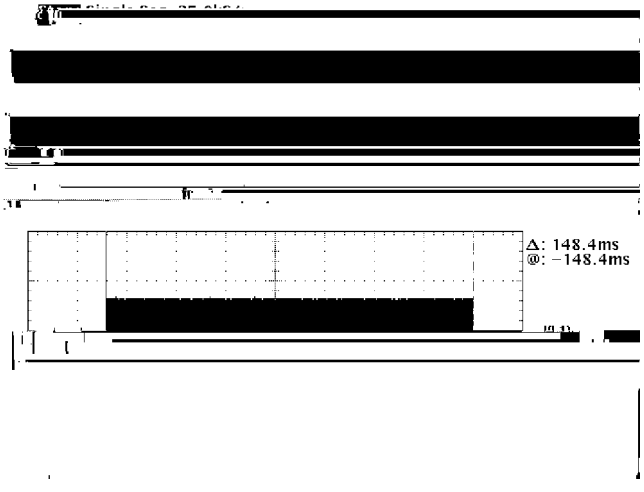


Figure 17. Overcurrent Shutoff (t_d = 160 ms)

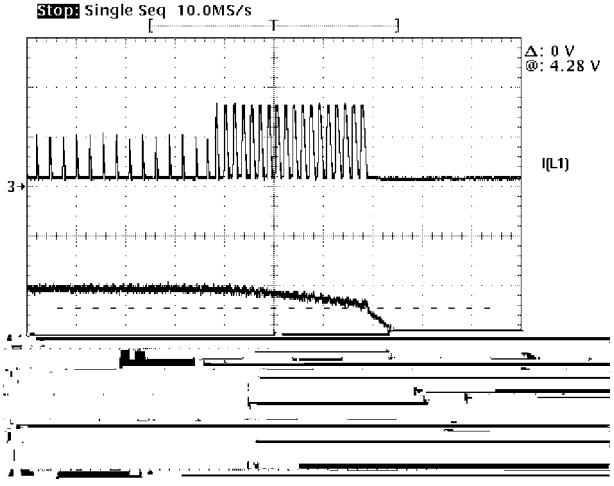


Figure 18. Undervoltage Shutoff (V_{T5L} = 4.6 V)

Table 1. PIN FUNCTION DESCRIPTION

Pin	Symbol	Type	Name/Function
CONTROLLER INTERFACE			
2	PWRON	INPUT Pulldown	This pin is used to start operation of the internal DC−DC converter. In programming mode, this pin is used to set the “Output Voltage” switch. (See Table 2).
3	INT	OUTPUT Pullup	This open collector pin indicates a change in the card presence circuit status. When a card is inserted or extracted, the pin goes to logic level “0”. The signal is reset to logic level “1” upon the rising edge of $\overline{CS}$ or upon the rising edge of PWRON. In the case of a multislot application, two or more $\overline{INT}$ outputs are connected together and the microcontroller has to poll all the MC33560s to identify which slot was detected.
4	RDYMOD	I/O and Pullup	This bidirectional pin has tri−state output and Schmitt trigger input. * When RDYMOD is forced to 0, the MC33560 can be set to programming mode by a negative transition on $\overline{CS}$. * When RDYMOD is connected to a high impedance, the MC33560 is in normal operating mode, and RDYMOD is in output mode (See Tables 2 and 4): − With $\overline{CS}$ = L and PWRON=H, RDYMOD indicates the status of the DC−DC converter. − With $\overline{CS}$ = L and PWRON=L, RDYMOD indicates the status of the card detector.
5	CS	INPUT Pullup	This is the MC33560 chip select signal. Pins 2, 6, 7, 10, 20, 21 are disabled when $\overline{CS}$ = H. When RDYMOD = L, the MC33560 enters programming mode upon the falling edge of $\overline{CS}$.

CARD V_{CC} AND CARD CLOCK PROGRAMMING

The $CRDV_{CC}$ and ASYCLK programming options allow the system clock frequency to be matched to the card clock frequency and to select 3.0 V or 5.0 V $CRDV_{CC}$ supply. Table 3 shows the values of **PWRON**, **RESET** and **I/O** for the possible options. The default power reset condition is state 4 (synchronous clock and $CRDV_{CC}$ =5.0 V). All states are latched for each output variable in programming mode at the positive transition of $\overline{\textbf{CS}}$ (Figure 20).

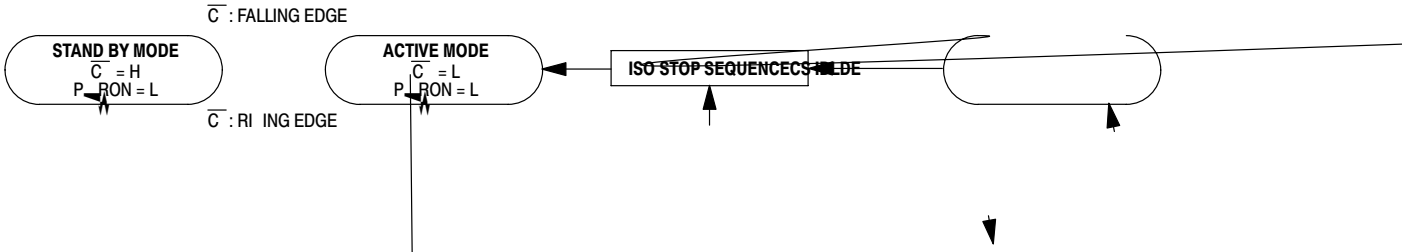


Figure 21. MC33560 Operating Modes

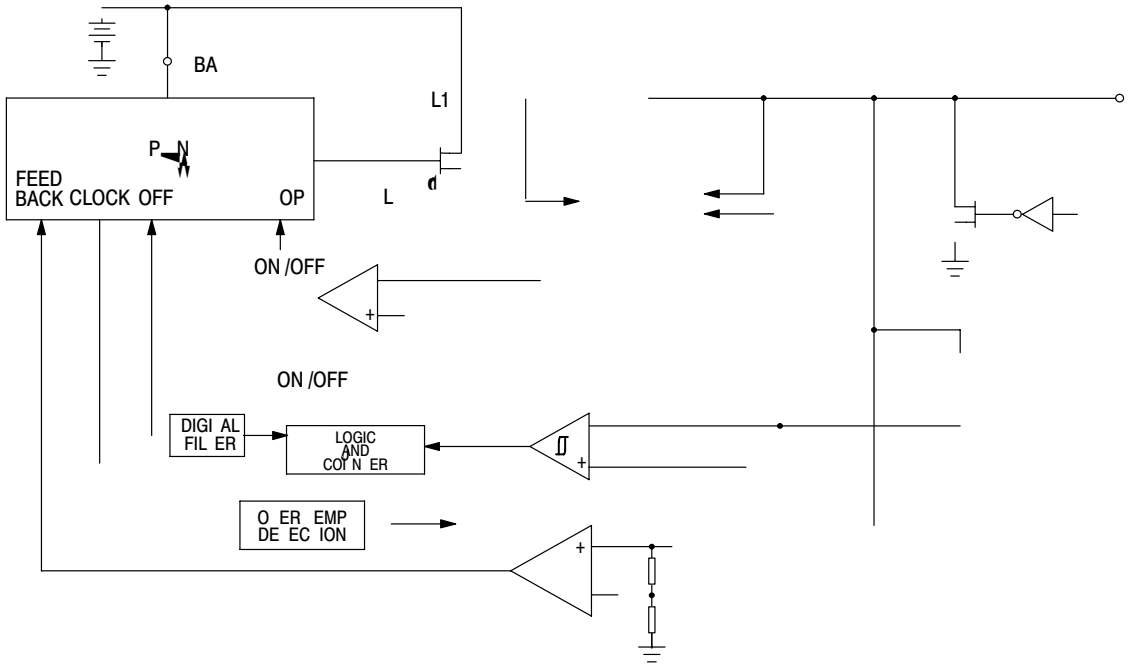


Figure 22. DC−DC Converter Functional Block

First, determine the maximum current that the application requires to supply to the card (ICCmax, on the y−axis)

BIDIRECTIONAL LEVEL TRANSLATOR

This module (used on **I/O/CRDIO**, **C4/CRDC4**, **C8/CRDC8**, Figure 24) adapts the signal voltage levels of the I/O and control lines between the micro controller (supplied by V_{BAT}) and the smartcard (supplied by $CRDV_{CC}$)

When $\overline{\textbf{CS}}$ is low, with $\textbf{CRDV}_{\textbf{CC}}$ on, and start sequencing completed, this module is transparent for the data, and acts as if the card was directly connected to the reader microcontroller. The core of the level shifter circuit defined for the bidirectional **CRDIO**, **CRDC4** and **CRDC8** lines consists of a NMOS switch which can be driven to the logic low state from either side (microcontroller or card). If both sides work in transmission mode with opposite phase, then signal collision on the line is not avoidable. In this case, the peak current is limited to a safe value for the integrated circuit and the smartcard.

During high−to−low transitions, the NMOS transistor impedance (T1 = 250 Ω maximum) is low enough to charge parasitic capacitance, and have a high enough dv/dt. On low to high transition, the NMOS transistor is not active above a certain voltage, and an acceleration circuit is activated to ensure a high dv/dt.

When the chip is disabled ($\overline{\textbf{CS}}$ = **H**) with the voltage supply $\textbf{CRDV}_{\textbf{CC}}$ still active, the **I/O**, **C4** and **C8** lines keep their last logic state.

When

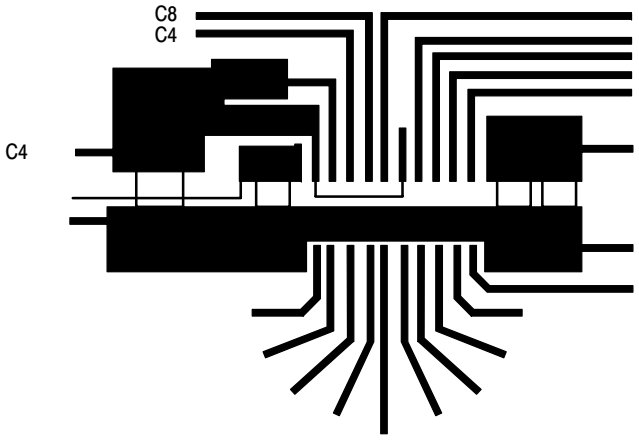
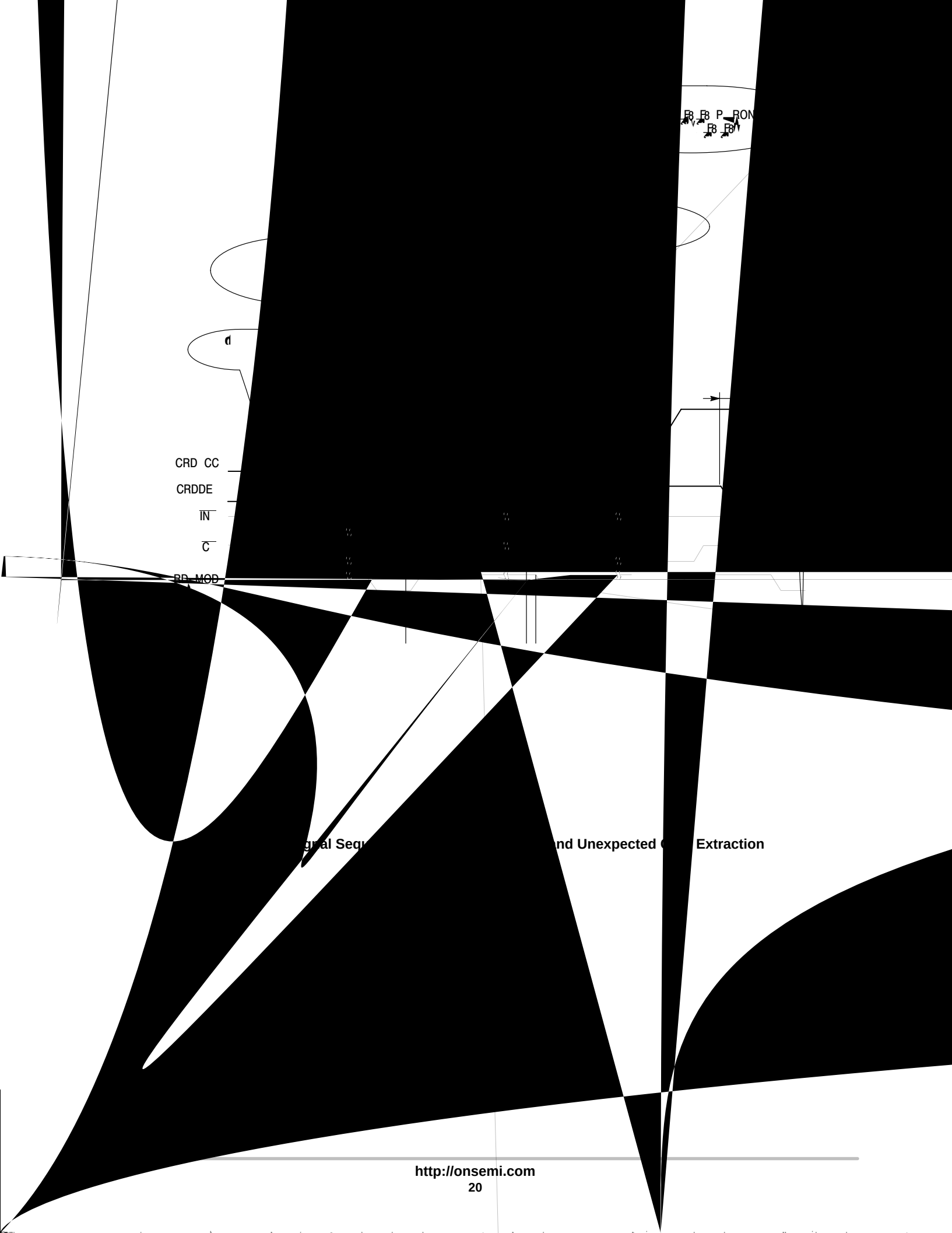


Figure 25. Example of Single Sided PCB Layout for MC33560



gnal Seq nd Unexpected C Extraction

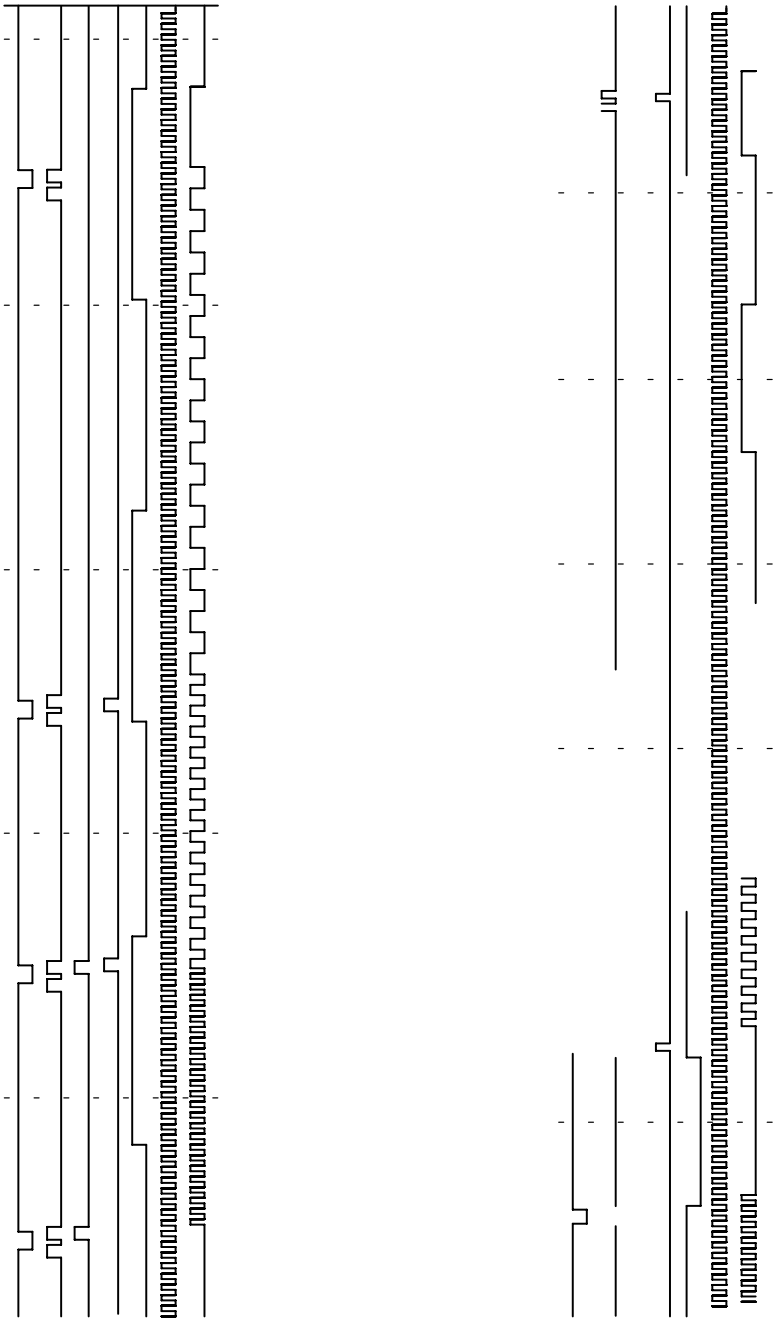


Figure 29. “On−the−Fly” Card Clock Selection Examples

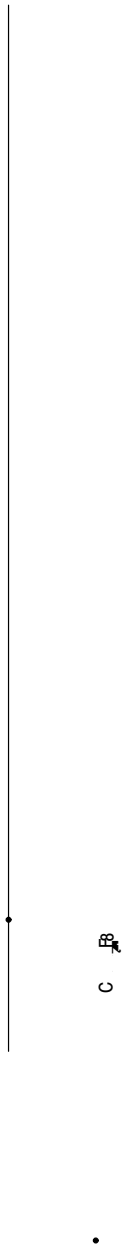
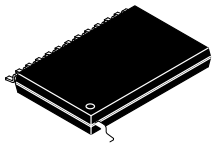


Figure 30. Card Reader/Writer Application

ORDERING INFORMATION

Device	Package	Shipping†
MC33560DTB	TSSOP−24	62 Units / Rail
MC33560DTBR2	TSSOP−24	2500 / Tape & Reel
MC33560DTBR2G	TSSOP−24 (Pb−Free)	2500 / Tape & Reel
MC33560DW	SO−24	30 Units / Rail
MC33560DWR2	SO−24	1000 / Tape & Reel
MC33560DWR2G	SO−24 (Pb−Free)	1000 / Tape & Reel



SCALE 2:1

TSSOP24 WB
CASE 948K
ISSUE O

DATE 17 FEB 2000