



High Performance Silicon Gate CMOS

C74AC04, C74AC 04

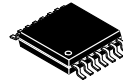
MARKING DIAGRAMS

Features

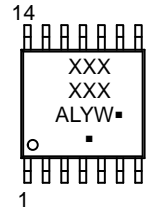
- Outputs Source/Sink 24 mA
- ACT04 Has TTL Compatible Inputs
- These are Pb-Free Devices



SOIC 14
D SUFFIX
CASE 751A



TSSOP 14
DT SUFFIX
CASE 948G



- XXXX = AC or ACT
- A = Assembly Location
- WL or L = Wafer Lot
- Y = Year
- WW or W = Work Week
- G or ■ = Pb-Free Package

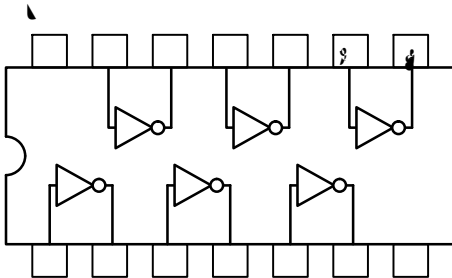


Figure 1. Pinout: 14 Lead Packages Conductors
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

MC74AC04, MC74ACT04

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq V_{CC} + 0.5$	V
V_O	DC Output Voltage (Note 1)	$-0.5 \leq V_O \leq V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 50	mA
I_O	DC Output Sink/Source Current	± 50	mA
I_{CC}	DC Supply Current per Output Pin	± 50	mA
I_{GND}	DC Ground Current per Output Pin	± 50	mA

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC	Unit	Conditions
			T _A = +25 C		T _A = 40 C to +85 C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = -50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0	-	2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} -24 mA -24 mA
		4.5	-	3.86	3.76		
		5.5	-	4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0	-	0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5	-	0.36	0.44		
		5.5	-	0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5	-				

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DC CHARACTERISTICS

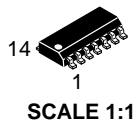
Symbol	Parameter	V _{CC} (V)	74ACT		74ACT	Unit	Conditions
			T _A = +25 C		T _A = 40 C to +85 C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		5.5	1.5	2.0	2.0		
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		5.5	1.5	0.8	0.8		
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA
		5.5	5.49	5.4	5.4		
		4.5	-	3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} -24 mA
		5.5	-	4.86	4.76		
V _{OL}	Maximum Low Level Output Voltage	4.5					

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DEVICE ORDERING INFORMATION

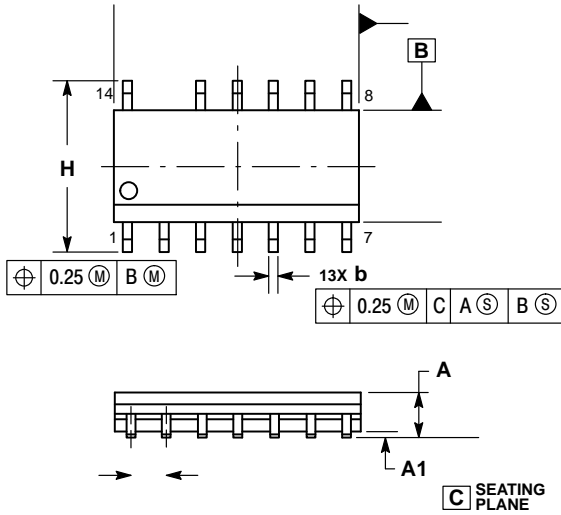
Device	Marking	Package	Shipping†
MC74AC04DG	AC04G	SOIC-14 (Pb-Free)	55 Units / Rail
MC74AC04DR2G	AC04G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74ACT04DR2G	ACT04G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74AC04DTR2G	AC 04	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
MC74ACT04DTR2G	ACT 04	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



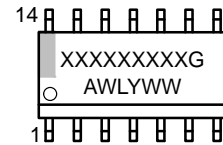
SOIC 14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

STYLES ON PAGE 2

SOIC 14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE

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