



# Quad 2-Input AND Gate

## High-Performance Silicon-Gate CMOS

### MC74AC08, MC74ACT08

#### Features

- Outputs Source/Sink 24 mA
- 'ACT08 Has TTL Compatible Inputs
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC2

GND

CC

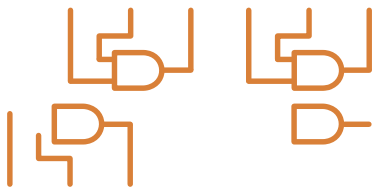


Figure .057c.68WRinout: 4q Tf1 0 0 9 0 71.3645 ND





# MC74AC08, MC74ACT08

## DC CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	74ACT		74ACT		Unit
				T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		
				Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage	V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V	4.5	1.5	2.0	2.0	V	
			5.5	1.5	2.0	2.0		
V <sub>IL</sub>	Maximum Low Level Input Voltage	V <sub>OUT</sub> = 0.1 V	4.5	1.5	0.8	0.8	V	

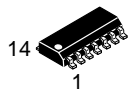
## MC74AC08, MC74ACT08

### ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74AC08DG	AC08	SOIC-14 (Pb-Free)	55 Units / Rail
MC74AC08DR2G	AC08	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74AC08DR2G-Q*	AC08	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74AC08DTR2G	AC 08	TSSOP-14 (Pb-Free)	2500 / Tape & Reel
MC74ACT08DG	ACT08	SOIC-14 (Pb-Free)	55 Units / Rail
MC74ACT08DR2G	ACT08	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74ACT08DTR2G	ACT 08	TSSOP-14 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

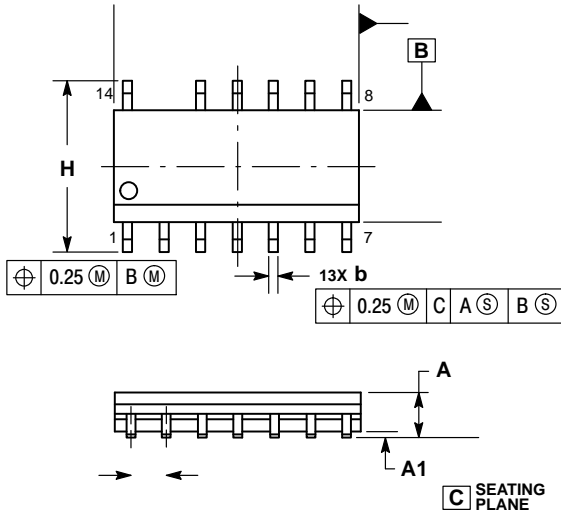
\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.



SCALE 1:1

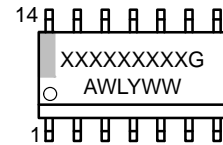
**SOIC 14 NB**  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
  5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

**GENERIC MARKING DIAGRAM\***



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

STYLES ON PAGE 2

**SOIC 14**  
CASE 751A-03  
ISSUE L

DATE 03 FEB 2016

STYLE 7:  
PIN 1. ANODE/CATHODE  
2. COMMON ANODE  
3. COMMON CATHODE  
4. ANODE/CATHODE  
5. ANODE/CATHODE





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