

Low-Voltage CMOS Hex Buffer with Open Drain Outputs

With 5 V-Tolerant Inputs

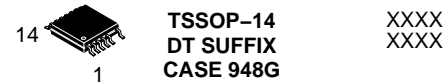
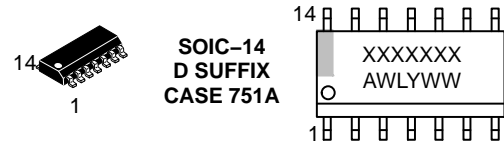
MC74LCX07

The MC74LCX07 is a high performance hex buffer operating from a 1.65 to 5.5 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers. These LCX devices have open drain outputs which provide the ability to set output levels, or do active HIGH AND or active LOW OR functions. A V_I specification of 5.5 V allows MC74LCX07 inputs to be safely driven from 5.0 V devices.

Features

- Designed for 1.65 to 5.5 V V_{CC} Operation
- 5.0 V Tolerant Inputs/Outputs
- LVTTL Compatible
- LVC MOS Compatible
- 24 mA Output Sink Capability @ 3.0 V
- Near Zero Static Supply Current (10 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- Wired OR, Wired AND
- Output Level Can Be Set Externally Without Affecting Speed of Device
- ESD Performance: Human Body Model >2000 V
- These Devices are Pb Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAMS



- XXXXXX = Specific Device Code
- A = Assembly Location
- L, WL = Wafer Lot
- Y, YY = Year
- W, WW = Work Week
- G or ■ = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

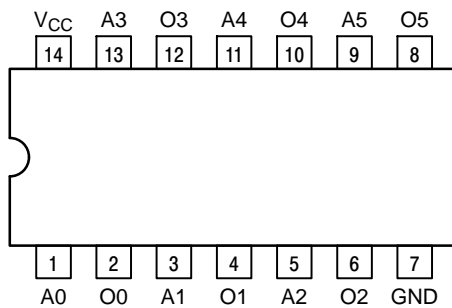


Figure 1. Pinout: 14-Lead (Top View)

MC74LCX07

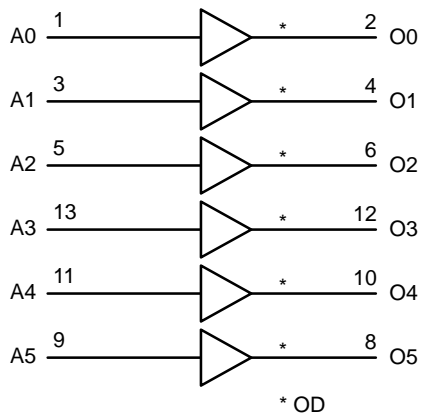


Figure 2. Logic Diagram

PIN NAMES

Pins	Function
An On	Data Inputs Outputs

TRUTH TABLE

An	On
L H	L Z

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V
V_I	DC Input Voltage (Note 1)	-0.5 to +6.5	V
V_O	DC Output Voltage (Note 1) Active-Mode (High or Low State) Tri-State Mode Power-Down Mode ($V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +6.5 -0.5 to +6.5	V
I_{IK}	DC Input Diode Current $V_I < GND$	-50	mA
I_{OK}	DC Output Diode Current $V_O < GND$	-50	mA
I_O	DC Output Source/Sink Current	± 50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin	± 100	mA
T_{STG}	Storage Temperature Range	-65 to +150	C
T_L	Lead Temperature, 1 mm from Case for 10 secs	260	C
T_J	Junction Temperature Under Bias		

MC74LCX07

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	Operating	1.65	3.3	5.5	V
		Data Retention Only	1.5	3.3	5.5	
V _I	Digital Input Voltage	0	–	5.5	V	
V _O	Output Voltage	Active Mode (High or Low State)	0	–	V _{CC}	V
		Tri-State Mode	0	–	5.5	
		Power Down Mode (V _{CC} = 0 V)	0	–	5.5	
T _A	Operating Free-Air Temperature	–40	–	+125	C	
t _r , t _f	Input Rise or Fall Rate	V _{CC} = 1.65 V to 1.95 V	0	–	20	nS/V
		V _{CC} = 2.3 V to 2.7 V	0	–	20	
		V _I from 0.8 V to 2.0 V, V _{CC} = 3.0 V	0	–	10	
		V _{CC} = 4.5 V to 5.5 V	0	–	5	

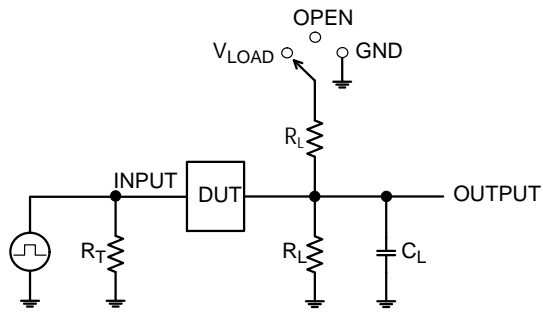
Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = –40°C to +85°C		T _A = –40°C to +125°C		Unit
				Min	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage		1.65 – 1.95	0.65 x V _{CC}	–	0.65 x V _{CC}	–	V
			2.3 – 2.7	1.7	–	1.7	–	
			3.0 – 3.6	2.0	–	2.0	–	
			4.5 – 5.5	0.70 x V _{CC}	–	0.70 x V _{CC}	–	
V _{IL}	LOW Level Input Voltage		1.65 – 1.95	–	0.35 x V _{CC}	–	0.35 x V _{CC}	V
			2.3 – 2.7	–				

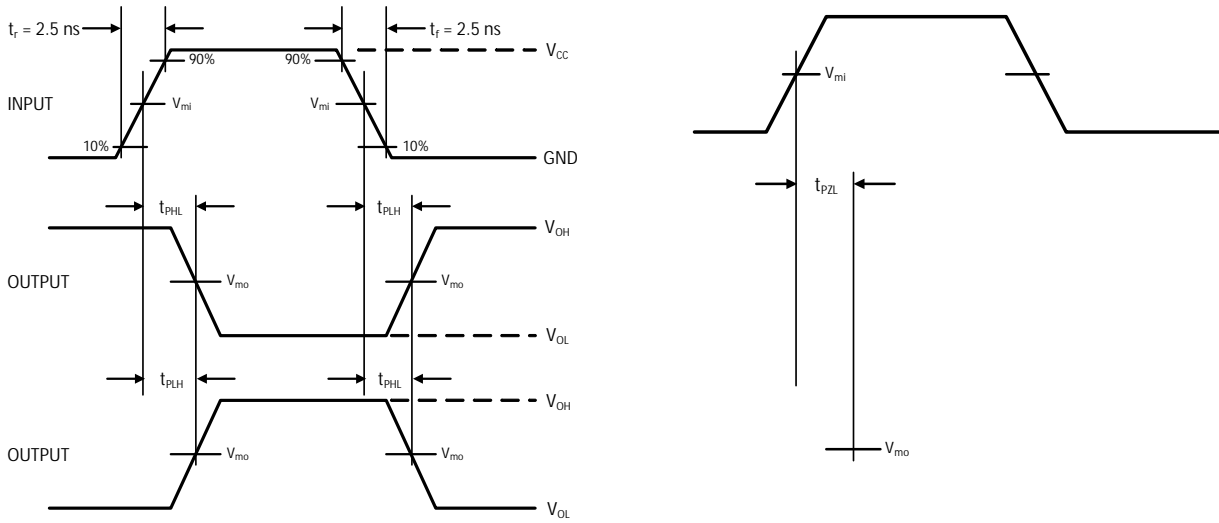
MC74LCX07

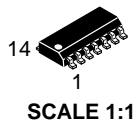


C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50Ω)
 $f = 1 \text{ MHz}$

Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND

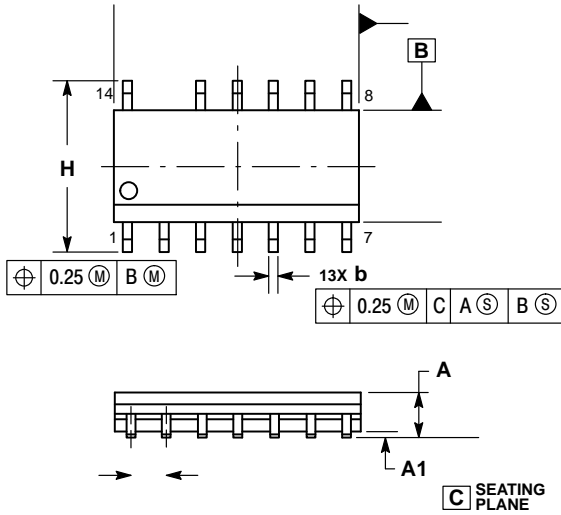
Figure 3. Test Circuit





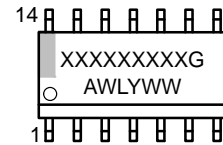
SOIC 14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

STYLES ON PAGE 2

SOIC 14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE

onsemi, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**
