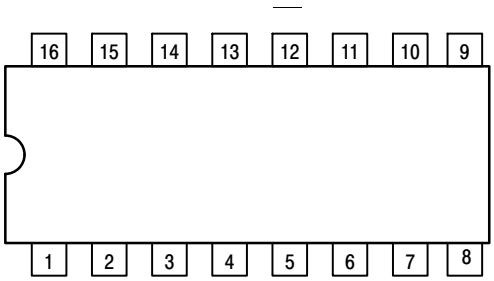


Figure 1. Pinout: 16−Lead (Top View)

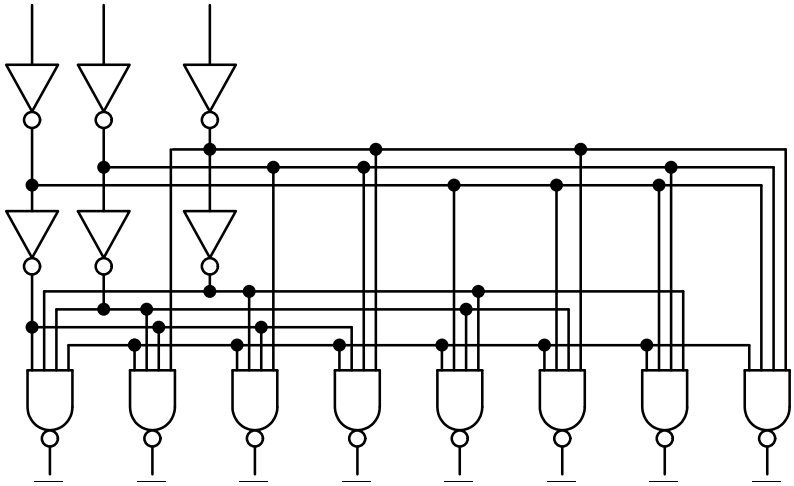


Figure 2. Logic Diagram

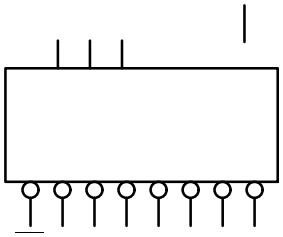
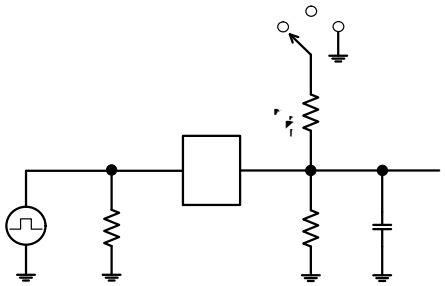


Figure 3. Expansion to 1−of−32 Decoding

RECOMMENDED OPERATING CONDITIONS

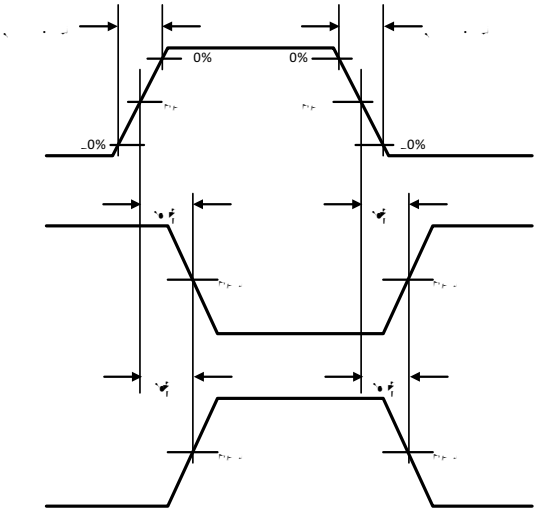
Symbol	Parameter	Min



Test	Switch Position

Ω

Figure 4. Test Circuit



ORDERING INFORMATION

Device	Marking	Package	Shipping

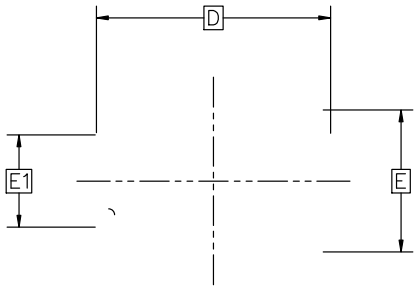
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.1[illegible]

nm TOTAL IN EXCESS OF THE

b DIMENSION AT MAXIMUM MATE

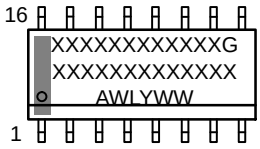


TOP VIEW

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

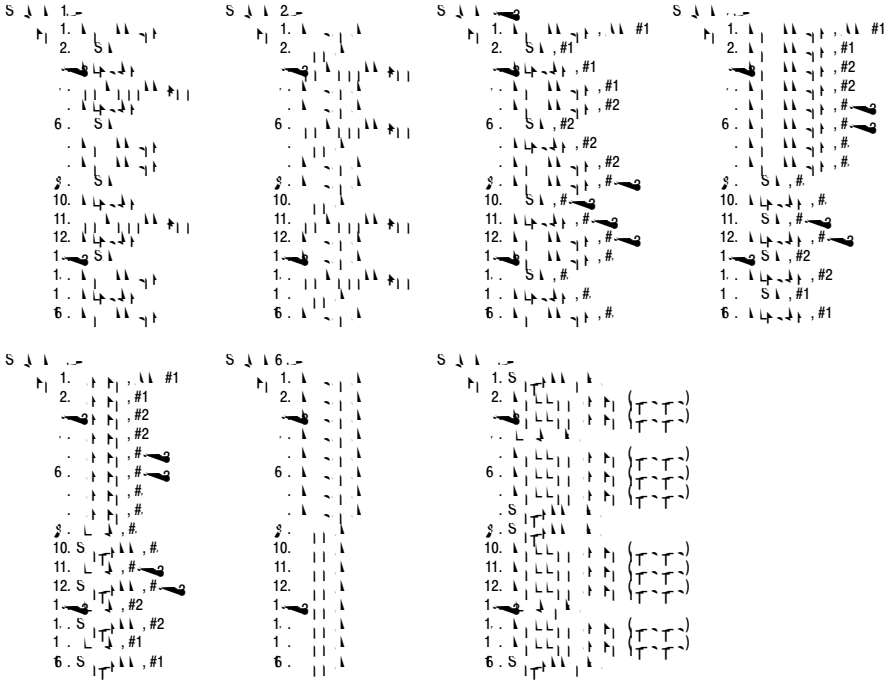
DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 2 OF 2**

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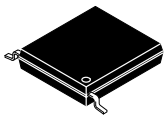

SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006

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