



# LATCH CMOS OUTPUT

## With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

### MC74LC 373

The MC74LCX373 is a high performance, non-inverting octal transparent latch operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5 V allows MC74LCX373 inputs to be safely driven from 5 V devices.

The MC74LCX373 contains 8 D-type latches with 3-state outputs. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present at the Dn input.

# MC74LCX373

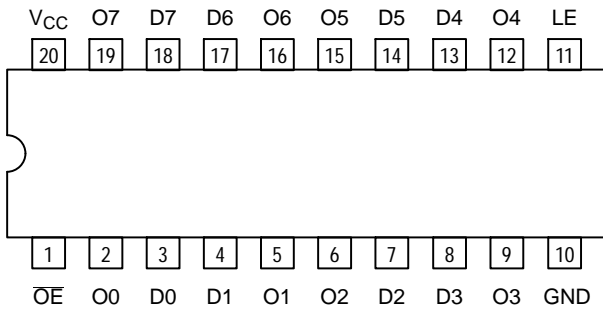


Figure 1. Pinout (Top View)

## PIN NAMES

PINS	FUNCTION
OE	Output Enable Input
LE	Latch Enable Input
D0–D7	Data Inputs
O0–O7	3–State Latch Outputs

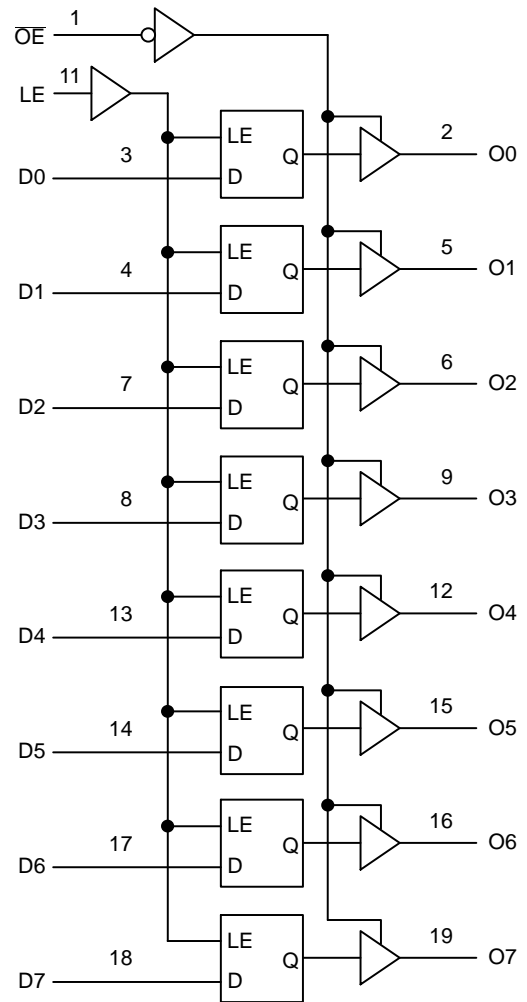


Figure 2. Logic Diagram

## TRUTH TABLE

INPUTS			OUTPUTS	OPERATING MODE
OE	LE	Dn	On	
L	H	H	H	Transparent (Latch Disabled); Read Latch
L	H	L	L	
L	L	h	H	Latched (Latch Enabled) Read Latch
L	L	l	L	
L	L	X	NC	Hold; Read Latch
H	L	X	Z	Hold; Disabled Outputs
H	H	H	Z	Transparent (Latch Disabled); Disabled Outputs
H	H	L	Z	
H	L	h	Z	Latched (Latch Enabled); Disabled Outputs
H	L	l	Z	

H = High Voltage Level

h = High Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition

L = Low Voltage Level

l = Low Voltage Level One Setup Time Prior to the Latch Enable High-to-Low Transition

NC = No Change, State Prior to the Latch Enable High-to-Low Transition

X = High or Low Voltage Level or Transitions are Acceptable

Z = High Impedance State

For I<sub>CC</sub> Reasons DO NOT FLOAT Inputs



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## DC ELECTRICAL CHARACTERISTICS

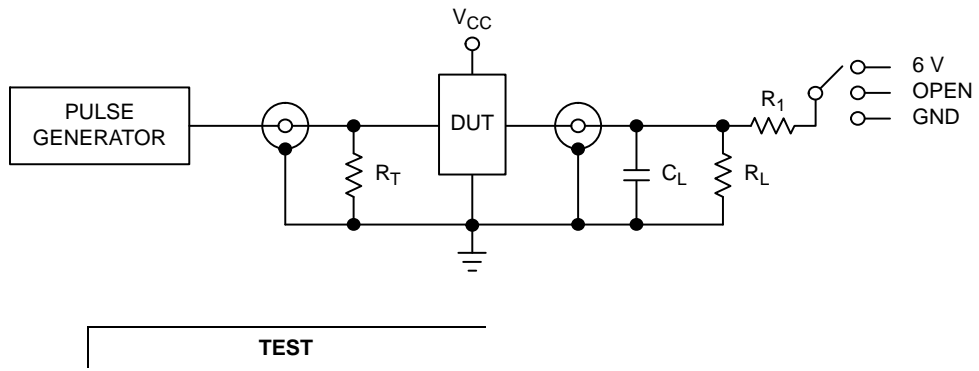
Symbol	Characteristic	Condition	T <sub>A</sub>
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V	
		2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V	
V <sub>IL</sub>	LOW Level Input Voltage (Note 2)	2.3 V ≤ V <sub>CC</sub> V	

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## DYNAMIC SWITCHING CHARACTERISTICS

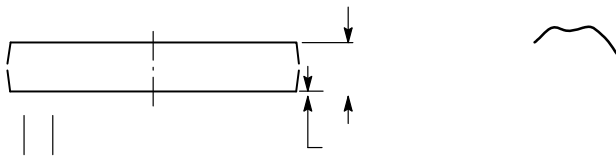
Symbol	Characteristic	Condition	T <sub>A</sub> = +25°C			Units
			Min	Typ	Max	
V <sub>OLP</sub>	Dynamic LOW Peak Voltage (Note 4)	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V V <sub>CC</sub> = 2.5 V, C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V		0.8 0.6		V
V <sub>OLV</sub>	Dynamic LOW Valley Voltage (Note 4)	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V V <sub>CC</sub> = 2.5 V, C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V				V

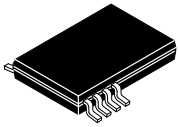
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SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015





SCALE 2:1

**TSSOP-20 WB**  
CASE 948E  
ISSUE D

DATE 17 FEB 2016



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