

With 5V-Tolerant Inputs

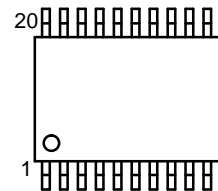
# MC74LVX373

The MC74LVX373 is an advanced high speed CMOS octal latch with 3 state outputs. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

This 8 bit D type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

### Features

- High Speed:  $t_{PD} = 5.8 \text{ ns (Typ)}$  at  $V_{CC} = 3.3 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 4 \mu\text{A (Max)}$  at  $T_A = 25 \text{ }^\circ\text{C}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise:  $V_{OLP} = 0.8 \text{ V (Max)}$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- These Devices are Pb Free and are RoHS Compliant



### PIN NAMES

| Pins            | Function              |
|-----------------|-----------------------|
| $\overline{OE}$ | Output Enable Input   |
| LE              | Latch Enable Input    |
| D0-D7           | Data Inputs           |
| O0-O7           | 3-State Latch Outputs |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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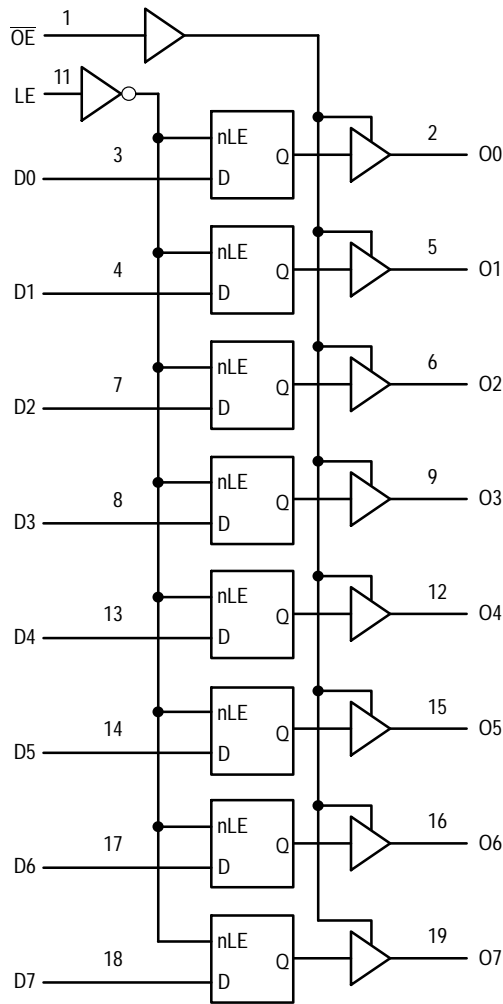


Figure 1. Logic Diagram

| INPUTS          |    |    | OUTPUTS | OPERATING MODE                                 |
|-----------------|----|----|---------|--|
| $\overline{OE}$ | LE | Dn | On      |  |
| L               | H  | H  | H       | Transparent (Latch Disabled); Read Latch       |
| L               | H  | L  | L       |  |
| L               | L  | h  | H       | Latched (Latch Enabled) Read Latch             |
| L               | L  | l  | L       |  |
| L               | L  | X  | NC      | Hold; Read Latch                               |
| H               | L  | X  | Z       | Hold; Disabled Outputs                         |
| H               | H  | H  | Z       | Transparent (Latch Disabled); Disabled Outputs |
| H               | H  | L  | Z       |  |
| H               | L  | h  | Z       | Latched (Latch Enabled); Disabled Outputs      |
| H               | L  | l  | Z       |  |

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## MAXIMUM RATINGS

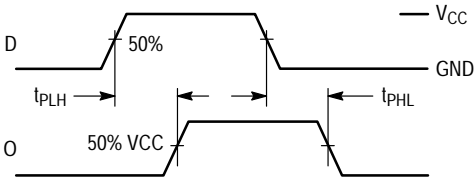
| Symbol    | Parameter                                | Value                  | Unit |
|-----------|--|------------------------|------|
| $V_{CC}$  | DC Supply Voltage                        | -0.5 to +7.0           | V    |
| $V_{in}$  | DC Input Voltage                         | -0.5 to +7.0           | V    |
| $V_{out}$ | DC Output Voltage                        | -0.5 to $V_{CC} + 0.5$ | V    |
| $I_{IK}$  | Input Diode Current                      | -20                    | mA   |
| $I_{OK}$  | Output Diode Current                     | 20                     | mA   |
| $I_{out}$ | DC Output Current, per Pin               | 25                     | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins | 75                     | mA   |
| $P_D$     |  |                        |      |

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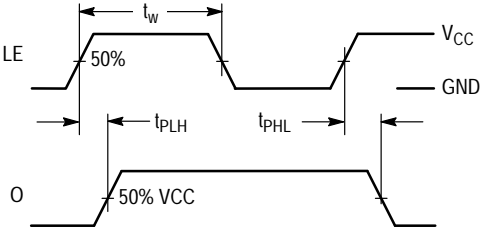
## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0ns$ )

| Symbol | Parameter | Test Conditions | T <sub>A</sub> = 25 C | T <sub>A</sub> = -40 to 85 C | Unit |
|--------|-----------|-----------------|-----------------------|------------------------------|------|
|--------|-----------|-----------------|-----------------------|------------------------------|------|

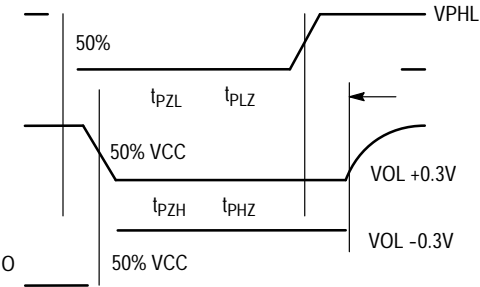
**MC74LVX373**



**Figure 2.**

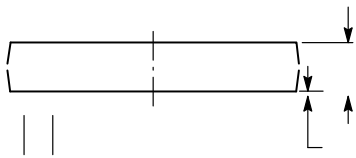


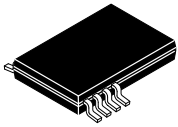
**Figure 3.**



SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015





SCALE 2:1

**TSSOP-20 WB**  
CASE 948E  
ISSUE D

DATE 17 FEB 2016

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