onsemi

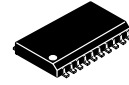**With 5 V−Tolerant Inputs**

C74L 573

SOIC−20
DW SUFFIX
CASE 751D

The MC74LVX573 is an advanced high speed CMOS octal latch with 3 state outputs. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

This 8 bit D type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

Features

High Speed: t_{PD} = 6.4 ns (Typ) at V_{CC} = 3.3 V

Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25 C

Power Down Protection Provided on Inputs

Balanced Propagation Delays

Low Noise: V_{OLP} = 0.8 V (Max)

Pin and Function Compatible with Other Standard Logic Families

Latchup Performance Exceeds 300 mA

ESD Performance: Human Body Model > 2000 V;
                  Machine Model > 200 V

These Devices are Pb Free and are RoHS Compliant

MARKING DIAGRAMS

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1
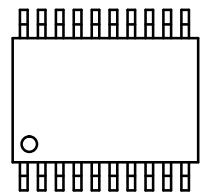
ORDERING INFORMATION

MC74LVX573

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	−40	+85	C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25 C Min	Typ	Max	T_A = −40 to 85 C Min	Max	Unit
V_{IH}	High−Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low−Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High−Level Output Voltage ($V_{in} = V_{IH}$ or V_{IL})	$I_{OH} = -50\ \mu A$ $I_{OH} = -50\ \mu A$ $I_{OH} = -4\ mA$	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low−Level Output Voltage ($V_{in} = V_{IH}$ or V_{IL})	$I_{OL} = 50\ \mu A$ $I_{OL} = 50\ \mu A$ $I_{OL} = 4\ mA$	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	$V_{in} = 5.5$ V or GND	3.6			0.1		1.0	μA
I_{OZ}	Maximum 3−State Leakage Current	$V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	3.6			0.25		2.5	μA
I_{CC}	Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	3.6						

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	$T_A = 25°C$			$T_A = -40$ to $85°C$		Unit
		Min	Typ	Max	Min	Max	
C_{in}	Input Capacitance		4	10		10	pF
C_{out}	Maximum 3–State Output Capacitance		6				pF
C_{PD}	Power Dissipation Capacitance (Note 2)		29				pF

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$ (per latch). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V, Measured in SOIC Package)

Symbol	Characteristic	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.5	−0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage			

SWITCHING WAVEFORMS
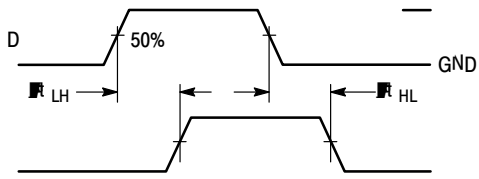
Figure 2.
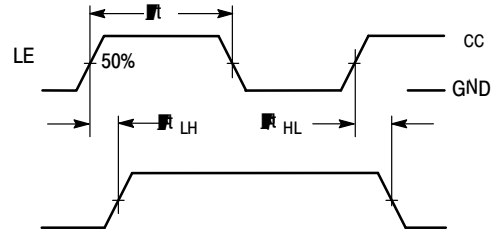
Figure 3.

Figure 4.

Figure 5.

DEVICE UNDER TEST

*Includes all probe and jig capacitance

DEVICE UNDER TEST

*Includes all probe and jig capacitance
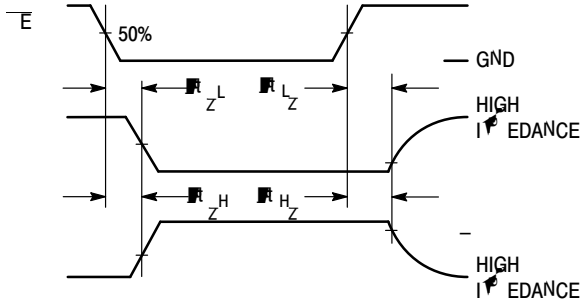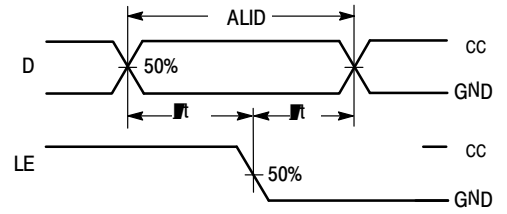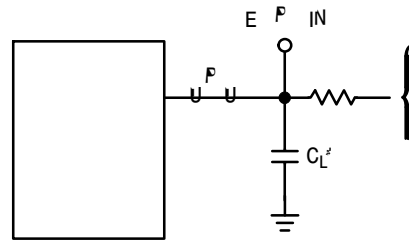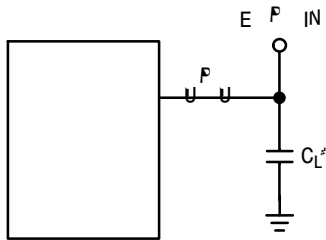
SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015
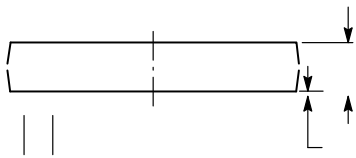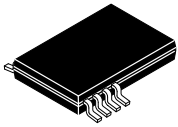
TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

SCALE 2:1