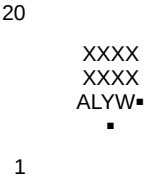
SOIC 20
DW SUFFIX
CASE 751D

TSSOP 20
DT SUFFIX
CASE 948E

MARKING DIAGRAMS



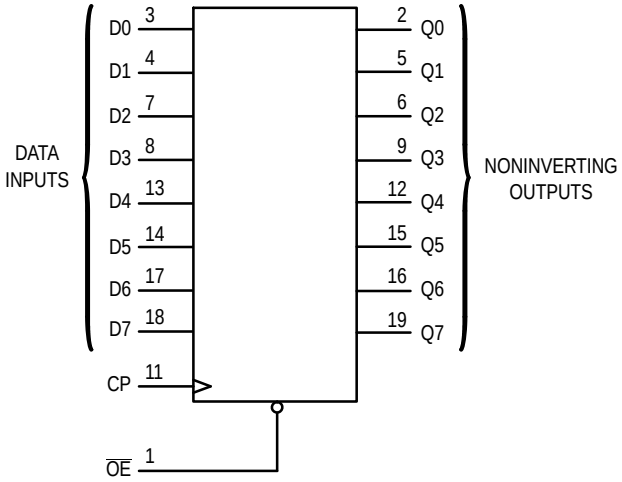


Figure 1. Logic Diagram

4. Tested to EIA/JESD78 Class II.

NOISE CHARACTERISTICS (MC74VHC374) (C_L = 50 pF, V_{CC} = 5.0 V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.6	0.9	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.6	−0.9	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS (MC74VHC374)

Symbol	Parameter	Test Conditions	T_A = 25°C		T_A = −40 to 85°C	Unit
			Typ	Limit	Limit	
t_w	Minimum Pulse Width, CP	V_{CC} = 3.3 ± 0.3 V V_{CC} = 5.0 ± 0.5 V		5.0 5.0	5.5 5.0	ns
t_{su}	Minimum Setup Time, D to CP	V_{CC} = 3.3 ± 0.3 V V_{CC} = 5.0 ± 0.5 V		4.5 3.0	4.5 3.0	ns
t_h	Minimum Hold Time, D to CP	V_{CC} = 3.3 ± 0.3 V V_{CC} = 5.0 ± 0.5 V		2.0 2.0	2.0 2.0	ns
t_r, t_f	Maximum Input Rise and Fall Times	V_{CC} = 3.3 ± 0.3 V V_{CC} = 5.0 ± 0.5 V				ns

DC ELECTRICAL CHARACTERISTICS (MC74VHCT374A)

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = −40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High−Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V_{IL}	Maximum Low−Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V_{OH}	Minimum High−Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = −50 μA	4.5	4.4	4.5		4.4		V
		I_{OH} = −8 mA	4.5	3.94			3.80		
V_{OL}	Maximum Low−Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50 μA	4.5		0.0	0.1		0.1	V
		I_{OL} = 8 mA	4.5			0.36		0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I_{OZ}	Maximum 3−State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			±0.25		±2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA
I_{CCT}	Quiescent Supply Current	Per Input: V_{IN} = 3.4 V Other Input: V_{CC} or GND	5.5			1.35		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5 V	0			0.5		5.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74VHCT374A)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = −40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 5.0 ± 0.5 V C_L = 15 pF C_L = 50 pF	90 85	140 130		80 95		MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CP to Q	V_{CC} = 5.0 ± 0.5 V C_L = 15 pF C_L = 50 pF		4.1 5.6	9.4 10.4	1.0 1.0	10.5 11.5	ns
t_{PZL}, t_{PZH}	Output Enable Time, $\overline{OE}$ to Q	V_{CC} = 5.0 ± 0.5 V C_L = 15 pF C_L = 50 pF		6.5 7.3	10.2 11.2	1.0 1.0	11.5 12.5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time $\overline{OE}$ to Q	V_{CC} = 5.0 ± 0.5 V C_L = 50 pF		7.0	11.2	1.0	12.0	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 5.0 ± 0.5 V C_L = 50 pF (Note 8)			1.0		1.0	ns
C_{in}	Maximum Input Capacitance			4	10		10	pF
C_{out}	Maximum 3−State Output Capacitance (Output in High−Impedance State)			9				pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 9)	25	pF

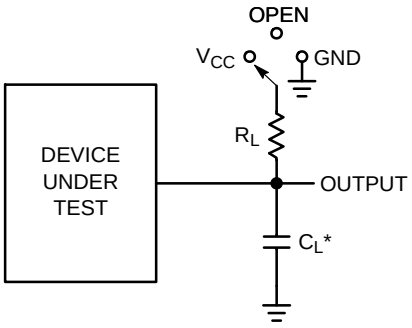
8. Parameter guaranteed by design. t_{OSLH} = $|t_{PLHm} - t_{PLHn}|$, t_{OSHL} = $|t_{PHLm} - t_{PHLn}|$.
9. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)}$ = C_{PD} • V_{CC} • f_{in} + I_{CC}/8 (per flip−flop). C_{PD} is used to determine the no−load dynamic power consumption; P_D = C_{PD} • V_{CC}^2 • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (MC74VHCT374A) (C_L = 50 pF, V_{CC} = 5.0 V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	1.2	1.6	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−1.6	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (MC74VHCT374A)

Symbol	Parameter	Test Conditions	T_A = 25°C		T_A = 40 to 85°C	Unit
			Typ	Limit	Limit	
t_w	Minimum Pulse Width, CP	V_{CC} = 5.0 ± 0.5 V		6.5	8.5	ns
t_{su}	Minimum Setup Time, D to CP	V_{CC} = 5.0 ± 0.5 V		2.5	2.5	ns
t_h	Minimum Hold Time, D to CP	V_{CC} = 5.0 ± 0.5 V		2.5	2.5	ns



*C_L Includes probe and jig capacitance
Input signal $t_R = t_F$ = 3 ns

Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	See AC	

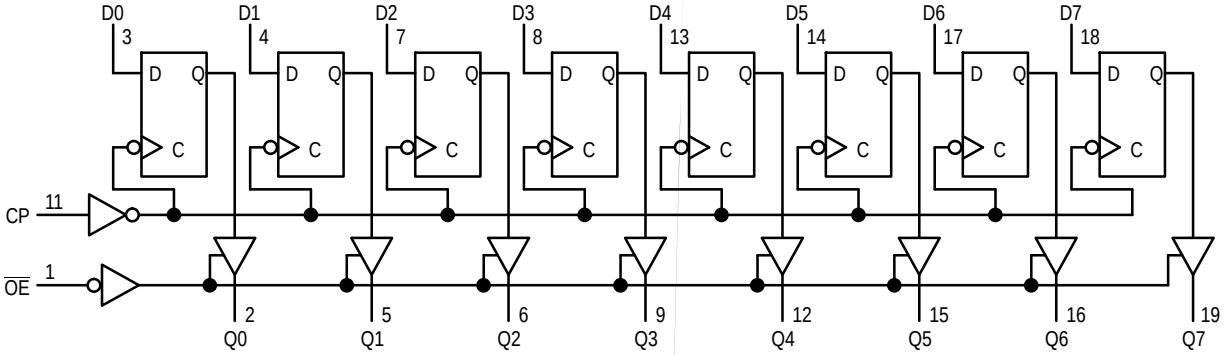


Figure 6. Expanded Logic Diagram

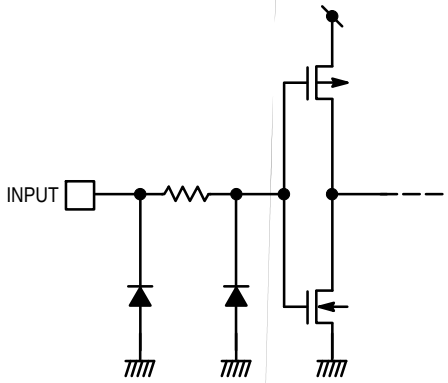


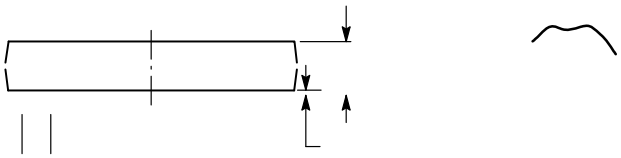
Figure 7. Input Equivalent Circuit

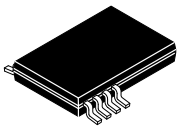
ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74VHC374DWR2G	VHC374G	SOIC−20W	1000 / Tape & Reel
MC74VHC374DTR2G	VHC 374	TSSOP−20	2500 / Tape & Reel
MC74VHCT374ADWR2G			

SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015





SCALE 2:1

TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016