DATA SHEET
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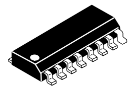


SOIC ï16
D SUFFIX
CASE 751B

MARKING DIAGRAMS

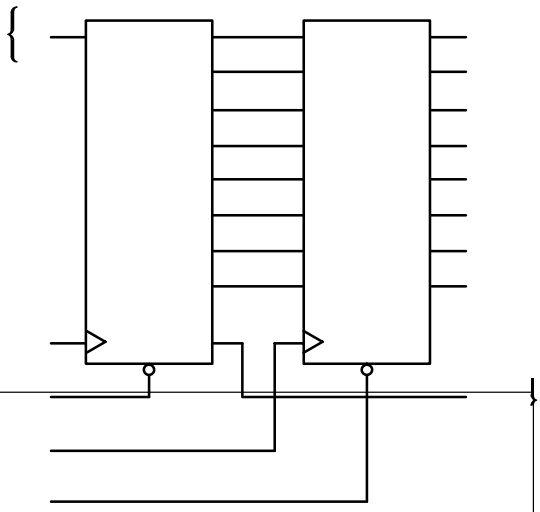
ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 10 of this data sheet.

€ These Devices are Pb-Free and are RoHS Compliant

Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

LOGIC DIAGRAM



FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset ($\overline{SCLR}$)	Serial Input (SI)	Shift Clock (SCK)	Reg Clock (RCK)	Output Enable ($\overline{OE}$)	Shift Register Contents	Storage Register Contents	Serial Output (SQH)	Parallel Outputs (QA ï QH)
Clear shift register	L	X	X	L, H,	L	L	U	L	U
Shift data into shift register	H	D		L, H,	L	D SR$_A$; SR$_N$ SR$_{N+1}$	U	SR$_G$ SR$_H$	U
Registers remains unchanged	H	X	L, H,	X	L	U	**	U	**
Transfer shift register contents to storage register	H	X	L, H,		L	U	SR$_N$ STR$_N$	*	SR$_N$
Storage register remains unchanged	X	X	X	L, H,	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled

Force outputs into high

im1E6803.68036BT5.364 re 182.5701860940.5629699Tm (X)Tj ET i9702 .62363 021.992 .680.754 im1 .6803 re f BT 7 .6803 re f BT 8 0 0 8Tj i9f

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage (Note 4)		0	5.5	V
V_{OUT}	DC Output Voltage (Note 4)		0	V_{CC}	V
T_A	Operating Temperature		–55	+125	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 3.0 V to 3.6 V V_{CC} = 4.5 V to 5.5 V	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			T_A = 85°C		T_A = 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High ïLevel Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low ïLevel Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V_{OH}	Minimum	V_{IN} = V_{IH} or V_{IL} I_{OH} = ï 50 A	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = ï									

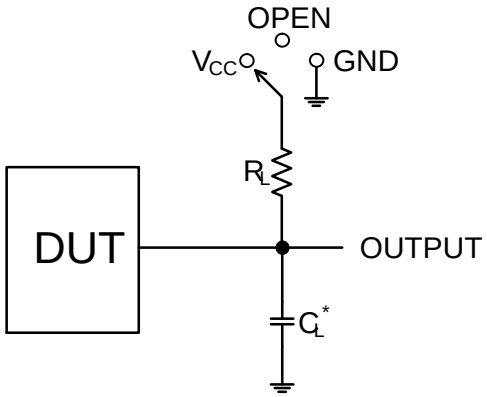
2.00E9D6280 51741e8661 32 9 48 641gh-1. re f 52.189273300ef>Vj f(1.35)Tj5 Tc (T43

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = 85°C		T_A = 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 3.3 ± 0.3 V	80	150		70		70		MHz
		V_{CC} = 5.0 ± 0.5 V	135	185		115		115		
t_{PLH}, t_{PHL}	Propagation Delay, SCK to SQH	V_{CC} = 3.3 ± 0.3 V C_L = 15pF		8.8	13.0	1.0	15.0	1.0	15.0	ns
		C_L = 50pF		11.3	16.5	1.0	18.5	1.0	18.5	
		V_{CC} = 5.0 ± 0.5 V C_L = 15pF		6.2	8.2	1.0	9.4	1.0	9.4	
		C_L = 50pF		7.7	10.2	1.0	11.4	1.0	11.4	
t_{PHL}	Propagation Delay, $\overline{CPLR}$ to SQH	V_{CC} = 3.3 ± 0.3 V C_L = 15pF		8.4	12.8	1.0	13.7	1.0	13.7	ns
		C_L = 50pF		10.9	16.3	1.0	17.2	1.0	17.2	
		V_{CC} = 5.0 ± 0.5 V C_L = 15pF		5.9	8.0	1.0	9.1	1.0	9.1	
		C_L = 50pF		7.4	10.0	1.0	11.1	1.0	11.1	
t_{PLH}, t_{PHL}	Propagation Delay, RCK to QA ïQH	V_{CC} = 3.3 ± 0.3 V C_L = 15pF		7.7	11.9	1.0	13.5	1.0	13.5	ns
		C_L = 50pF		10.2	15.4	1.0	17.0	1.0	17.0	
		V_{CC} = 5.0 ± 0.5 V C_L = 15pF		5.4	7..4	1.0	8.5	1.0	8.5	
		C_L = 50pF		6.9	9.4	1.0	10.5	1.0	10.5	
t_{PZL}, t_{PZH}	Output Enable Time, $\overline{OE}$ to QA ïQH	V_{CC} = 3.3 ± 0.3 V C_L = 15pF		7.5	11.5	1.0	13.5	1.0	13.5	ns
		C_L = 50pF		9.0	15.0	1.0	17.0	1.0	17.0	
		V_{CC} = 5.0 ± 0.5 V C_L = 15pF		4.8	8.6	1.0	10.0	1.0	10.0	
		C_L = 50pF		8.3	10.6	1.0	12.0	1.0	12.0	
t_{PLZ}, t_{PHZ}	Outp0t Ore f (= 3701 T8 358 .6803 2570.8963 480.586 2093.222222 45H149 .68Ee f BT Tm -.0025 Tc (= 15pF)Tj034 68022H Tc (C)Tj 6.5 0 0 6.5 2.077									

TIMING REQUIREMENTS

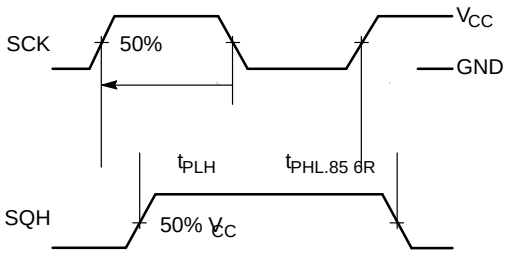
Symbol	Parameter	V_{CC} V	T_A = 25°C		T_A = ï 40 to 85°C	T_A = ï 55 to 125°C	Unit
			Typ	Limit	Limit	Limit	
t_{su}	Setup Time, SI to SCK	3.3 5.0		3.5 3.0	3.5 3.0	3.5 3.0	ns
$t_{su(H)}$	Setup Time, SCK to RCK	3.3 5.0		8.0 5.0	8.5 5.0	8.5 5.0	ns
$t_{su(L)}$	Setup Time, $\overline{SCLR}$ to RCK	3.3 5.0		8.0 5.0	9.0 5.0	9.0 5.0	ns
t_h	Hold Time, SI to SCK	3.3 5.0		1.5 2.0	1.5 2.0	1.5 2.0	ns
$t_{h(L)}$	Hold Time, $\overline{SCLR}$ to RCK	3.3 5.0		0 0	0 0	1.0 1.0	ns
t_{rec}	Recovery Time, $\overline{SCLR}$ to SCK	3.3 5.0		3.0 2.5	3.0 2.5	3.0 2.5	ns
t_w	Pulse Width, SCK or RCK	3.3 5.0		5.0 5.0	5.0 5.0	5.0 5.0	ns
$t_{w(L)}$	Pulse Width, $\overline{SCLR}$	3.3 5.0		5.0 5.0	5.0 5.0	5.0 5.0	ns

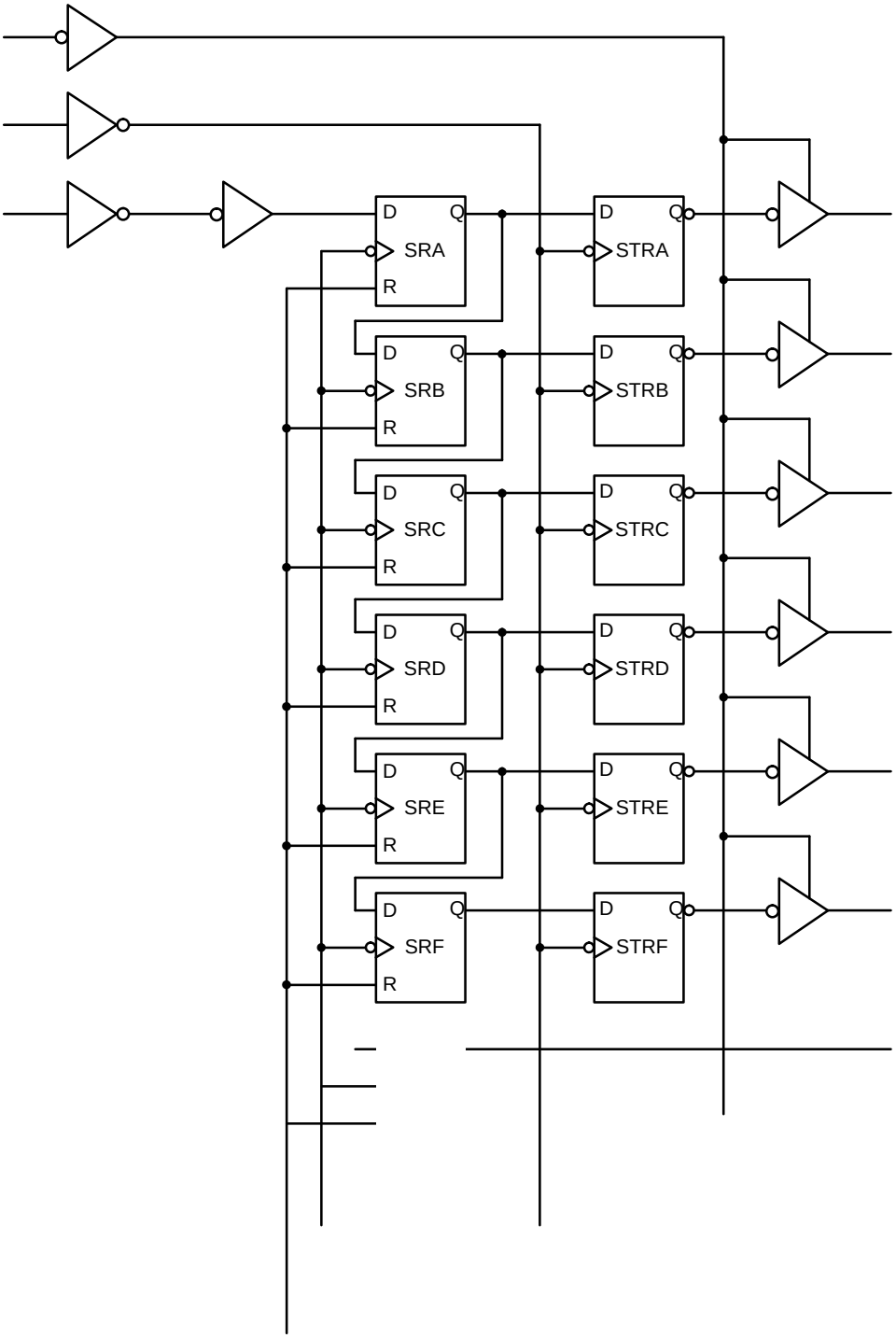


Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table	1 k
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

*C_L Includes probe and jig capacitance
Input t_R = t_F = 3 ns

Figure 1. Test Circuit




D
Q
SRA
R
STRA
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SRE
STRE
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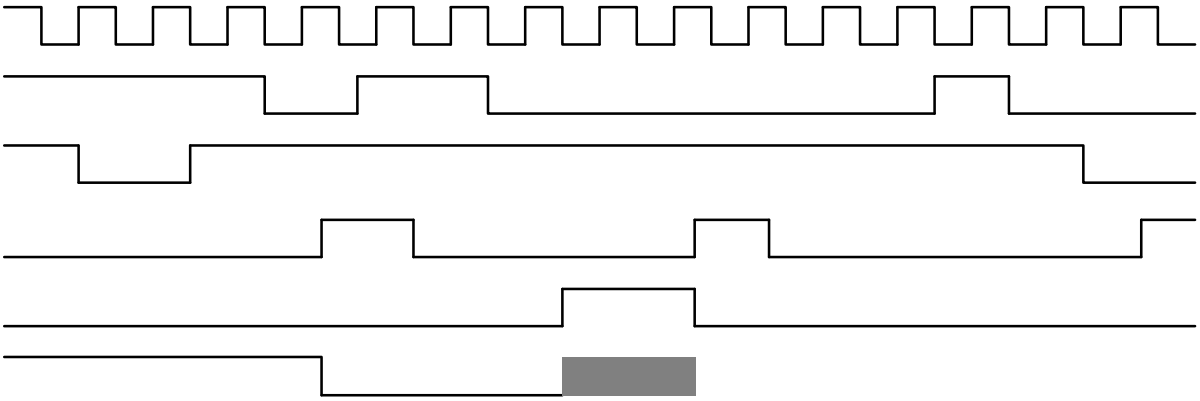
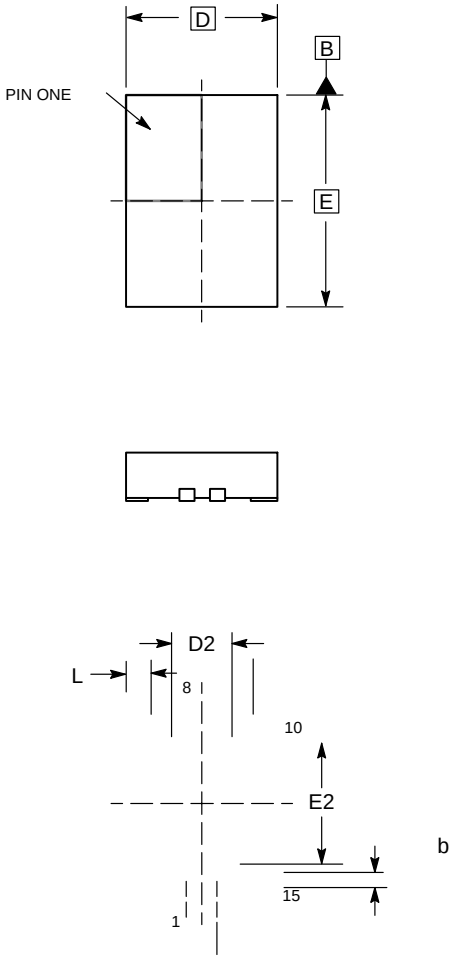


PACKAGE DIMENSIONS

QFN16, 2.5x3.5, 0.5P
CASE 485AW
ISSUE O

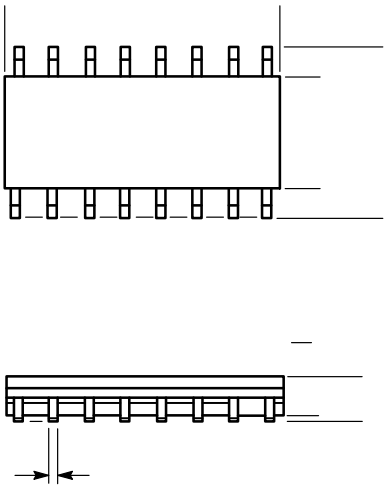


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A		
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2		
e	0.50 BSC	
K	0.20	---

PACKAGE DIMENSIONS

SOIC ï16
CASE 751B ï05
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.