

## **Dual D-Type Flip-Flop with Set and Reset**

#### MARKING DIAGRAMS

#### SOIC-14

### MC74VHC74, MC74VHCT74A

The MC74VHC74 and MC74VHCT74A are high speed CMOS D Type Flip Flops fabricated with silicon gate CMOS technology. These achieve high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The signal level applied to the D input is transferred to Q output during the positive going transition of the Clock pulse.

Reset  $(\overline{RD})$  and Set  $(\overline{SD})$  are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

The MC74VHC74 inputs are compatible with standard CMOS levels while the MC74VHCT74A inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The MC74VHC74 and MC74VHCT74A internal circuits are composed of three stages, including a buffer output which provides high noise immunity and stable output. The input structures tolerate voltages up to 5.5 V, allowing the interface of 5 V systems to 3 V systems.

The MC74VHCT74A output structures provide protection when  $V_{CC}=0$  V. These output structures help prevent device destruction caused by supply voltage input/output voltage mismatch, battery backup, hot insertion, etc.

#### **Features**

High Speed:  $f_{max}$  (MC74VHC74) = 170 MHz (Typ) at  $V_{CC}$  = 5 V  $f_{max}$  (MC74VHCT74A) = 60 MHz (Typ) at  $V_{CC}$  = 5 V

Low Power Dissipation:  $I_{CC} = 2 \mu A$  (Max) at  $T_A = 25 C$ 

High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$ 

Power Down Protection Provided on Inputs

**Balanced Propagation Delays** 

Designed for 2.0 V to 5.5 V Operating Range

Low Noise:  $V_{OLP} = 0.8 \text{ V (Max)}$ 

Pin and Function Compatible with Other Standard Logic Families

Latchup Performance Exceeds 100 mA

ESD Performance:

Human Body Model > 2000 V

Chip Complexity: 128 FETs or 32 Equivalent Gates

Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC Q100 Qualified and PPAP Capable

These Devices are Pb Free, Halogen Free/BFR Free and are RoHS Compliant



#### **FUNCTION TABLE**

Inputs				Outputs	
SD	RD	CP	D	Q	Q
		_			
		_			
		_			
		~			

#### ORDERING INFORMATION

MC74VHC74, MC74VHCT74A				

www.onsemi.com

# D46 Tw3[mC

#### MC74VHC74, MC74VHCT74A

#### AC ELECTRICAL CHARACTERISTICS

			T <sub>A</sub> = 25 C		T <sub>A</sub> = -55 C to +125 C			
Symbol	Parameter	Test Conditions	Min	Тур	Max	Min	Max	Unit
	_							
			l		l			

#### MC74VHC74, MC74VHCT74A

#### DC ELECTRICAL CHARACTERISTICS

			v <sub>cc</sub>	T <sub>A</sub> = 25 C		T <sub>A</sub> = - 55 to 125 C			
Symbol	Parameter	Test Conditions	v	Min	Тур	Max	Min	Max	Unit
	-								
	-								

#### MC74VHC74, MC74VHCT74A

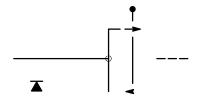
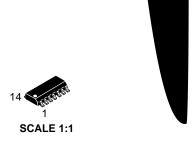
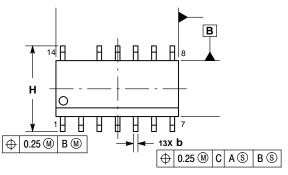


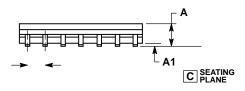
Figure 7. Input Equivalent Circuit

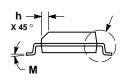


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#### **DATE 03 FEB 2016**







- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

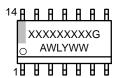
  2. CONTROLLING DIMENSION: MILLIMETERS.

  3. DIMENSION & DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.

  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.

  5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
- SIDE.

#### **GENERIC MARKING DIAGRAM\***



XXXXX = Specific Device Code Α = Assembly Location

WL= Wafer Lot Υ = Year WW = Work Week G = Pb-Free Package

**STYLES ON PAGE 2** 

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STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE

