onsemi

3-to-8 Line Decoder MC74VHCT138A

The MC74VHCT138A is an advanced high speed CMOS 3 to 8 decoder fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

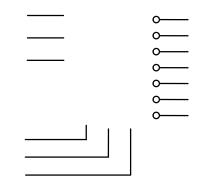
When the device is enabled, three Binary Select inputs (A0 A2) determine which one of the outputs ($\overline{Y0}$ $\overline{Y7}$) will go Low. When enable input E3 is held Low or either E2 or E1 is held High, decoding function is inhibited and all outputs go high. E3, E2, and E1 inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

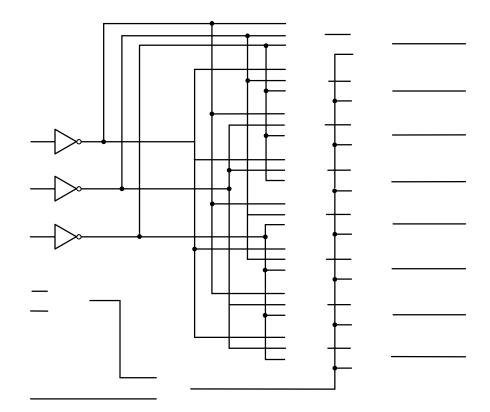
The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because they have full 5.0 V CMOS level output swings.

The VHCT138A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage input/output voltage mismatch, battery backup, hot insertion, etc.

Features

, andp008 033W(Features)Tj /TT3 1 Tf 12 0 0 13* -. 12h3 1 u111c.s.13.3 V(Fe2r1ePiu10 mdD Tc 0 Tw (: I70.2992 406.0 al



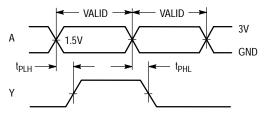


MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V _{in}	DC Input Voltage	– 0.5 to + 7.0	V
V _{out}	DC Output Voltage V _{CC} = 0 High or Low State	- 0.5 to + 7.0 - 0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	- 20	mA
I _{OK}	Output Diode Current ($V_{OUT} < GND; V_{OUT} > V_{CC}$)	20	mA
l _{out}	DC Output Current, per Pin	25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	75	mA
Р		-	-

25.852 refq59.754 593.348 38.268 -259 ref367 n0 792 2 -791.9846 Tc(În711336 8 73.4179C68 -259 r67 46.0913 592.2747 Tm0 g/T1 1 Tf.mA

SWITCHING WAVEFORMS





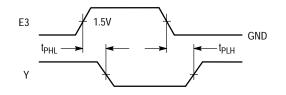
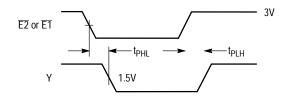


Figure 3.





*Includes all probe and jig capacitance

Figure 5. Test Circuit



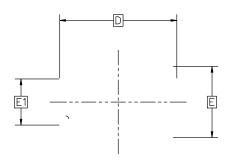
SOIC-16 9.90x3.90x1.37 1.27P CASE 751B ISSUE M

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- DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.1^r

b DIMENSION AT MAXIMUM MATE

nm TOTAL IN EXCESS OF THE



<u>top view</u>

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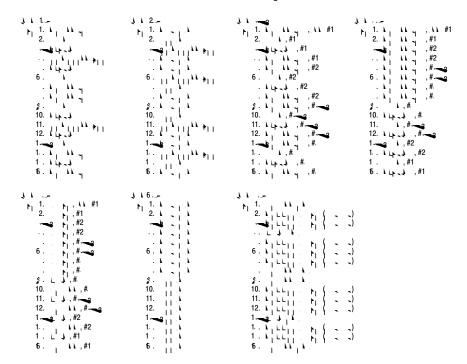
GENERIC MARKING DIAGRAM*

16	A	H	A.	- A	- A	A	A	E
		XX)	XX)	XX	XX)	XX)	XX	G
		XX	XX)	XX)	XX)	XX	XX)	x
	0	D AWLYWW						
1	Ŧ	<u> </u>	Н	H	H	Н	H	Ъ

XXXXX = Specific Device Code

- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



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