1 Mb Ultra-Low Power Serial SRAM

Standard SPI Interface and Multiplex DUAL and QUAD Interface

Overview

The ON Semiconductor serial SRAM family includes several integrated memory devices including this 1 Mb serially accessed Static Random Access Memory, internally organized as 128 K words by 8 bits. The devices are designed and fabricated using ON Semiconductor's advanced CMOS technology to provide both high-speed performance and low power. The devices operate with a single chip select ($\overline{CS}$) input and use a simple Serial Peripheral Interface (SPI) protocol. In SPI mode, a single data-in (SI) and data-out (SO) line is used along with the clock (SCK) to access data within the device. In DUAL mode, two multiplexed data-in/data-out (SIO0-SIO1) lines are used and in QUAD mode, four multiplexed data-in/data-out (SIO0-SIO3) lines are used with the clock to access the memory. The devices can operate over a wide temperature range of −40°C to +85°C (+125°C for E−Temp) and are available in a 8-lead TSSOP package. The N01S830xA device has two different variations, a HOLD version that allows communication to the device to be paused and a battery back-up (BBU) version to be used with a battery to retain data when power is lost.

Features

- Power Supply Range: 2.5 to 5.5 V
- Very Low Typical Standby Current < 4 μA at +85°C
- Very Low Operating Current < 10 mA
- Simple Serial Interface
  - Single-bit SPI Access
  - DUAL-bit and QUAD-bit SPI-like Access
- Flexible Operating Modes
  - Word Mode
  - Page Mode
  - Burst Mode (Full Array)
- High Frequency Read and Write Operation
  - Clock Frequency up to 20 MHz
- Functional Options
  - HOLD Pin for Pausing Operation
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Table 3. CONTROL SIGNAL DESCRIPTIONS

Signal	Mode Used	Name	Description
$\overline{HOLD}$	SPI and DUAL	Hold	A high level is required for normal operation. Once the device is selected and a serial sequence is started, this input may be taken low to pause serial communication without resetting the serial sequence. The pin must be brought low while SCK is low for immediate use. If SCK is not low, the HOLD function will not be invoked until the next SCK high to low transition. The device must remain selected during this sequence. SO is high-Z during the Hold time and SI and SCK are inputs are ignored. To resume operations, $\overline{HOLD}$ must be pulled high while the SCK pin is low. Lowering the $\overline{HOLD}$ input at any time will take to SO output to High-Z.
VBAT	SPI and DUAL	Battery Voltage	Provides the battery power connection to retain data in battery backed mode.
SIO0 - 1	DUAL	Serial Data Input / Output	Receives instructions, addresses and data on the rising edge of SCK. Data is transferred out after the falling edge of SCK. The instruction must be set after power-up to enable the DUAL access mode.
SIO0 - 3	QUAD	Serial Data Input / Output	Receives instructions, addresses and data on the rising edge of SCK. Data is transferred out after the falling edge of SCK. The instruction must be set after power-up to enable the QUAD access mode.

Basic Operation

The 1 Mb serial SRAM is designed to interface directly with a standard Serial Peripheral Interface (SPI) common on many standard micro-controllers in the default state. It may also interface with other non-SPI ports by programming discrete I/O lines to operate the device.

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The serial SRAM contains an 8-bit instruction register and is accessed via the SI pin. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation. Data is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared, the user can assert the $\overline{HOLD}$ input and place the device into a Hold mode. After releasing the $\overline{HOLD}$ pin, the operation will resume from the point where it was held. The Hold operation is only supported in SPI and DUAL modes.

By programming the device through a command instruction, the dual and quad access modes may be initiated. In these modes, multiplexed I/O lines take the place of the SPI SI and SO pins and along with the $\overline{CS}$ and SCK control the device in a SPI-like, two bit (DUAL) and four bit B

DEVICE OPERATIONS

Read Operation

The serial SRAM Read operation is started by by enabling $\overline{CS}$ low. First, the 8-bit Read instruction is transmitted to the device through the SI (or SIO0-3) pin(s) followed by the 24-bit address with the 7 MSBs of the address being “don’t care” bits and ignored. In SPI mode, after the READ instruction and address bits are sent, the data stored at that address in memory is shifted out on the SO pin after the output valid time. Additional “dummy” clock cycles (four in DUAL and two in QUAD) are required to follow the instruction and address inputs prior to the data being driven out on the SIO0-3 pins while operating in these two modes.

By continuing to provide clock cycles to the device, data can continue to be read out of the memory array in sequentially. The internal address pointer is automatically incremented to the next higher address after each byte of data is read out until the highest memory address is reached. When the highest memory address is reached, 1FFFFh, the address pointer wraps to the address 00000h. This allows the read cycles to be continued indefinitely. All Read operations are terminated by pulling $\overline{CS}$ high.

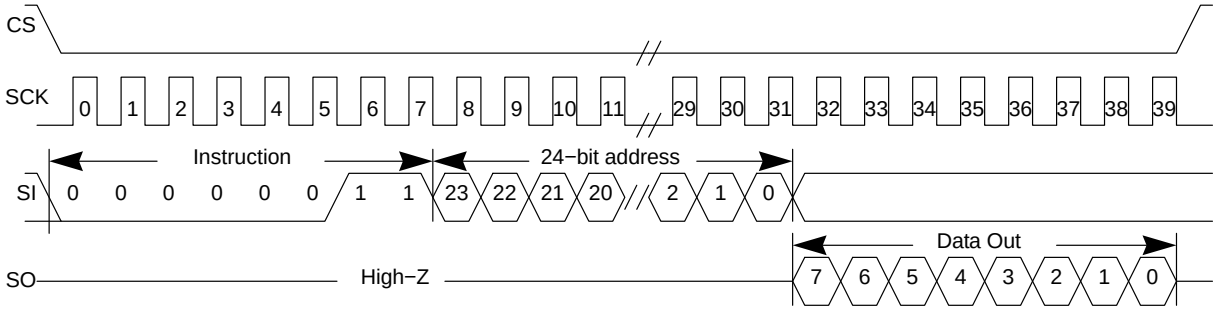


Figure 2. SPI Read Sequence (Single Byte)

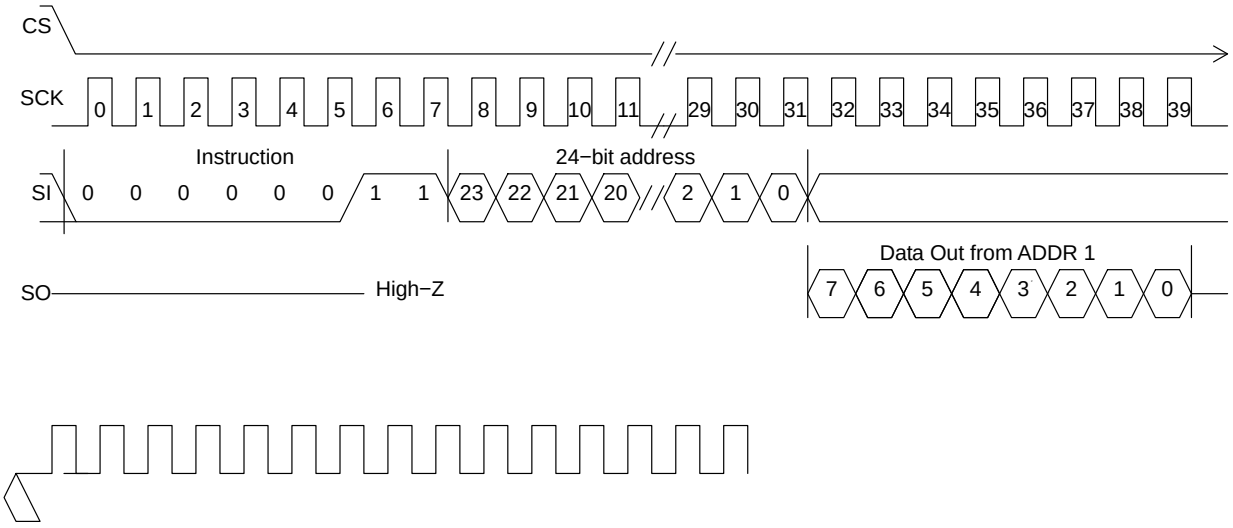


Figure 3. SPI Read Sequence (Sequential Bytes)

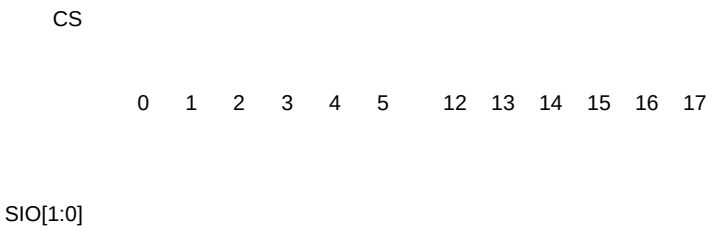


Figure 4. DUAL Read Sequence

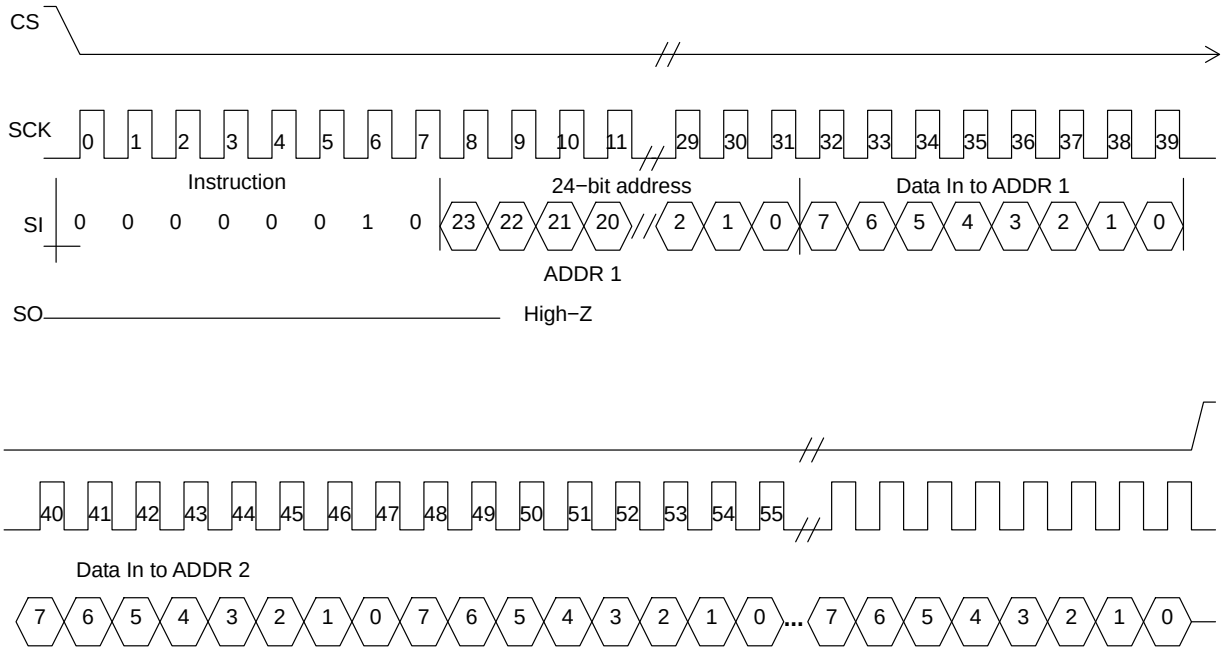
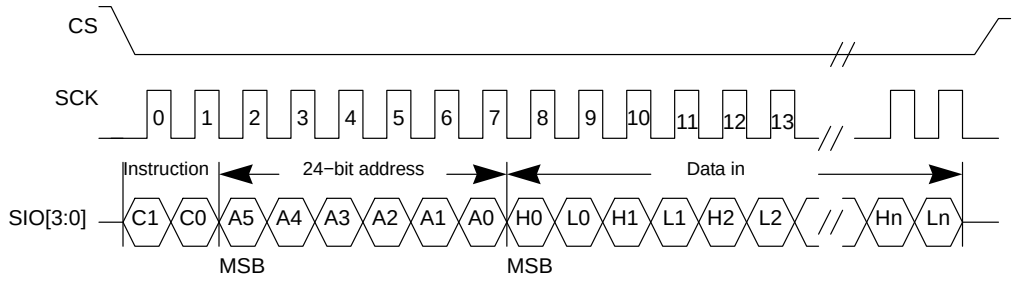


Figure 6. SPI Write Sequence



Notes: C[1:0] = 02h
H0 = 4 high order bits of data byte 0
L0 = 4 low order bits of data byte 0
H1 = 4 high order bits of data byte 1
L1 = 4 low order bits of data byte 1

Figure 8. QUAD Write Sequence

READ Mode Register (RDMR)

This instruction provides the ability to read the mode register. The register may be read at any time including during a Write operation. The Read Mode Register operation is executed by driving $\overline{CS}$ low, then sending the RDMR instruction to the device. Immediately after the instruction, the device outputs data on the SO (SIO0-3) pin(s). To complete the operation, drive $\overline{CS}$ high to terminate the register read.

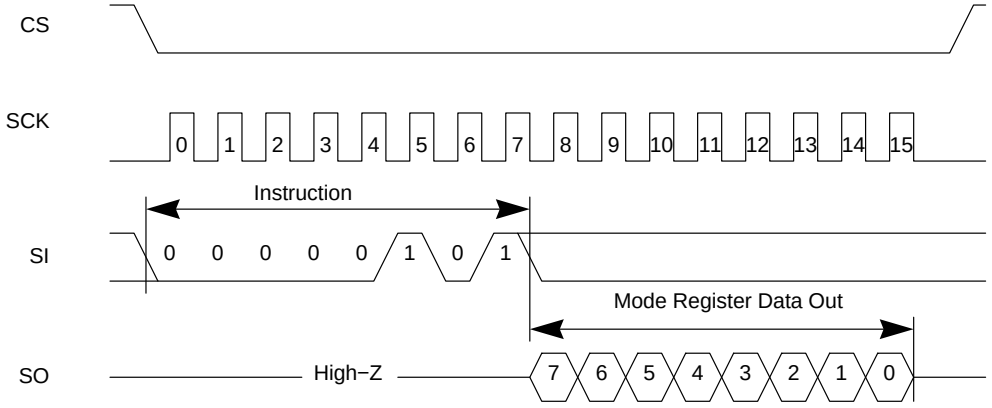
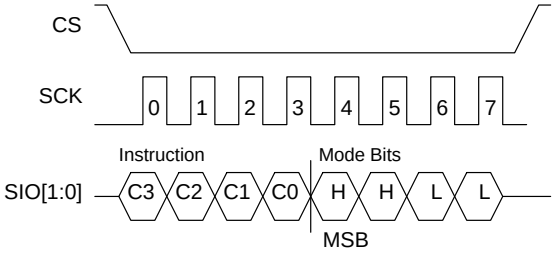
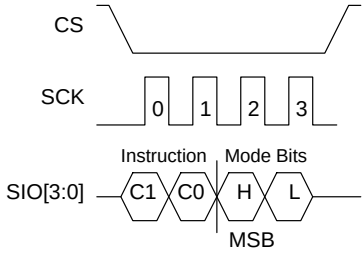


Figure 9. SPI Read Mode Register Sequence (RDMR)



Notes: C[3:0] = 05h

Figure 10. DUAL Read Mode Register Sequence (RDMR)



Notes: C[1:0] = 05h

Figure 11. QUAD Read Mode Register Sequence (RDMR)

Write Mode Register (WRMR)

This instruction provides the ability to write the mode register. The Write Mode Register operation is executed by driving $\overline{CS}$ low, then sending the WRMR instruction to the device. Immediately after the instruction, the data is driven to the device on the SO (SIO0-3) pin(s). To complete the operation, drive $\overline{CS}$ high to terminate the register write.

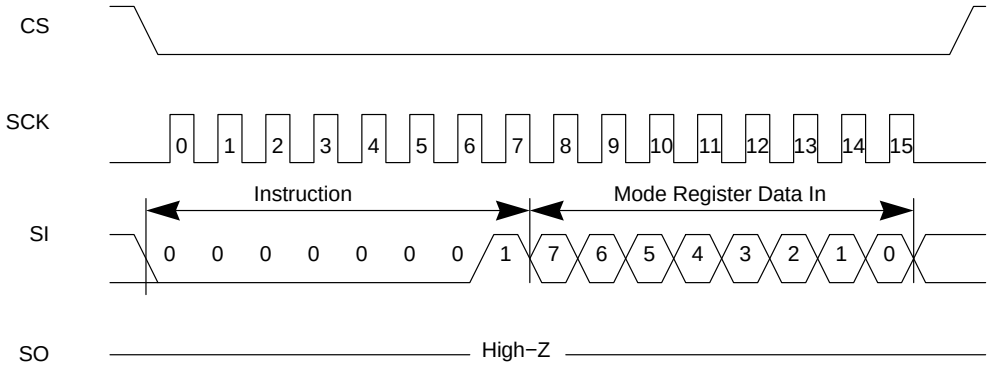
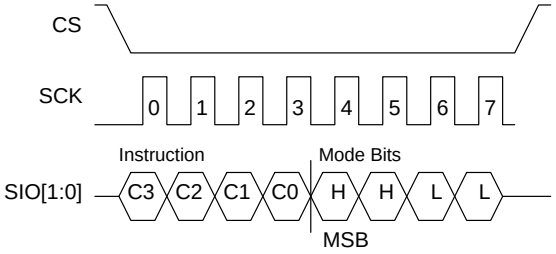
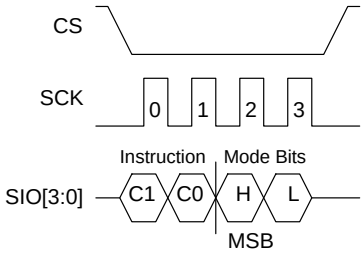


Figure 12. SPI Write Mode Register Sequence



Notes: C[3:0] = 01h

Figure 13. DUAL Write Mode Register Sequence



Notes: C[1:0] = 01h

Figure 14. QUAD Write Mode Register Sequence

Table 5. MODE REGISTER

Bit	Function
0	Hold Function 1 = Hold function disabled 0 = Hold function enabled (Default)
1	Reserved
2	Reserved
3	Reserved
4	Reserved
5	Reserved
6	Operating Mode Bit 7 Bit 6 0 0 = Word Mode 1 0 = Page Mode 0 1 = Burst Mode (Default) 1 1 = Reserved
7	

Power-Up State

The serial SRAM enters a know state at power-up time. The device is in low-power standby state with $\overline{CS}$ = 1. A low level on $\overline{CS}$ is required to enter a active state.

Battery Back-Up Operation

The Battery Back-Up function is available on the BBU version of the serial SRAM. This version of the SRAM cannot operate in the QUAD mode since the SIO3 input is used for the VBAT connection. A standard coin cell battery should be connected to the VBAT pin. On chip circuitry monitors the V_{CC} pin and when it is determined that the main V_{CC} power supply is turning off, the device automatically switches the memory array to VBAT power input. When in battery back-up mode and 3.0 to 3.4 V power supplied to the VBAT input, memory data is retained in the SRAM array and all existing interface and operating mode information is retained.

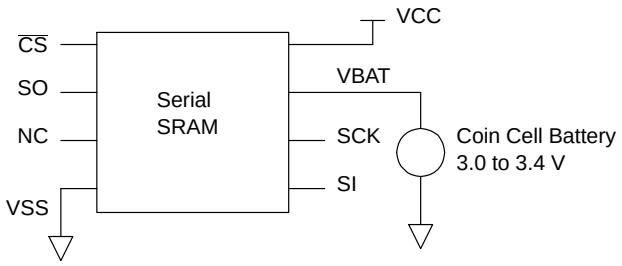


Figure 15. Battery Back-Up Version Schematics

Table 6. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC} + 0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 5.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	−40°C to 125°C	°C
Ambient Temperature Under Bias	T_A	−40°C to +125°C	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10 sec	°C

Stresses

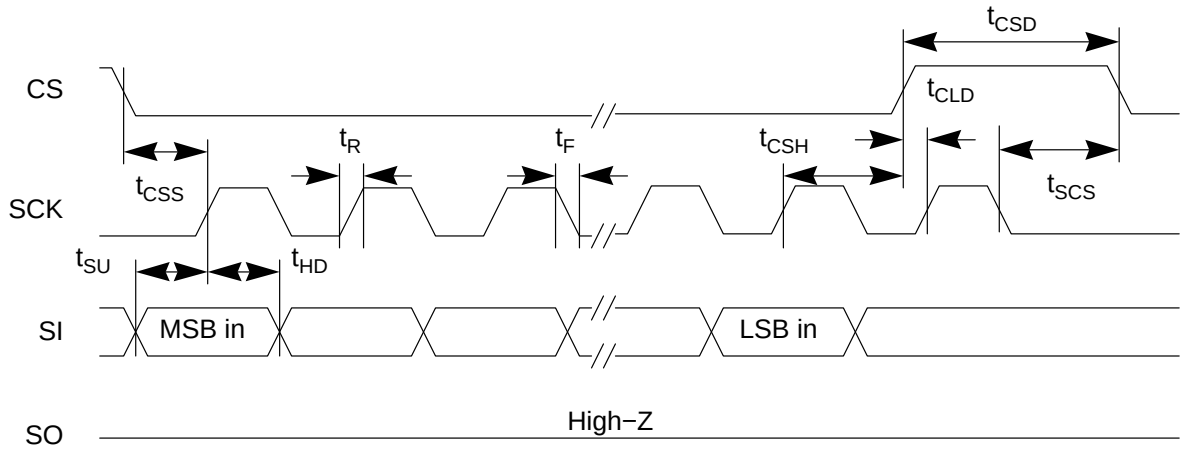


Figure 16. SPI Input Timing

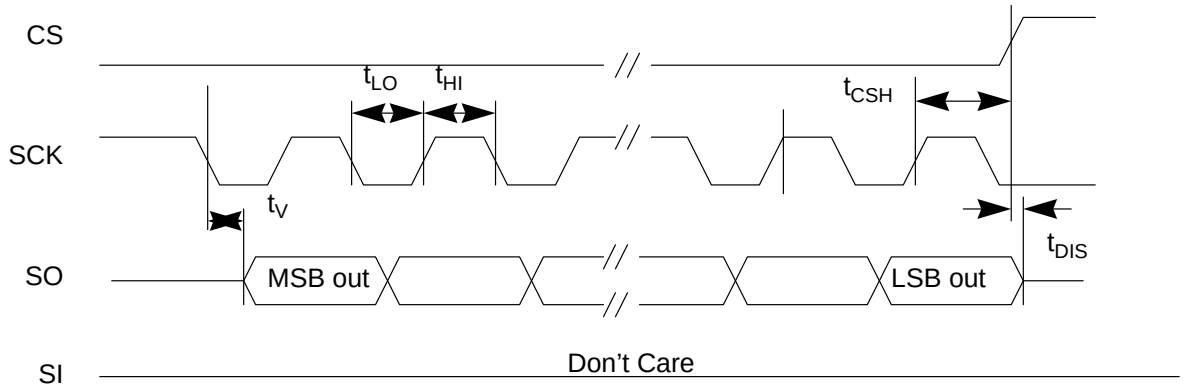


Figure 17. SPI Output Timing

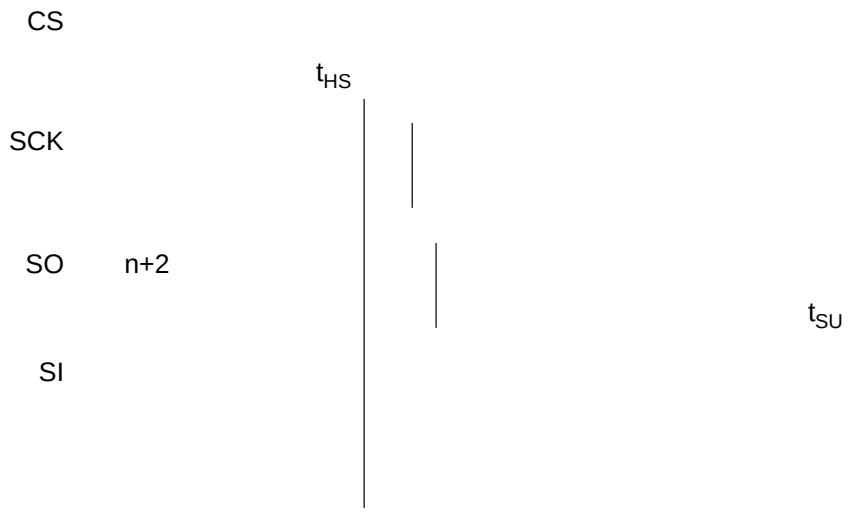


Figure 18. SPI Hold Timing

PACKAGE DIMENSIONS

TSSOP8 3x4.4 / TSSOP8 (225 mil)
CASE 948BH
ISSUE O