# nsemi

# 256 Kb I<sup>2</sup>C CMOS Serial EEPROM with Software Write Protect N24C256X

#### Description

The N24C256X is a 256 Kb Serial CMOS EEPROM, internally organized as 32,768 words of 8 bits each.

It features a 64 byte page write buffer and supports the Standard (100 kHz), Fast (400 kHz) and Fast Plus (1 MHz) I<sup>2</sup>C protocol.

The device also features a 128 bit factory set read only Unique ID and Software Write Protection of the entire array. The Unique ID may be used to identify the manufacturer and the device.

#### Features

- Supports Standard, Fast and Fast Plus I<sup>2</sup>C Protocol
- SCL and SDA Pins Operate at 1.2 V
- 1.7 V to 5.5 V Supply Voltage Range
- 64 Byte Page Write Buffer
- User Programmable Permanent Write Protection
- Schmitt Triggers and Noise Suppression Filters on I<sup>2</sup>C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Temperature Range: 40°C to +125°C
- Ultra thin 4 ball WLCSP Package
- This Device is Pb Free, Halogen Free/BFR Free and RoHS Compliant\*

\*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



WLCSP4 CASE 567XG

#### **PIN CONFIGURATION**



WLCSP4 1.00x1.00x0.30 (Top View)

#### **PIN FUNCTION**

Pin Name	Function
SDA	Serial Data Input/Output
SCL	Serial Clock Input
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground

#### MARKING DIAGRAM



X = Specific Device Code

- Y = Production Year (Last Digit)
- W = Production Work Week

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.



Figure 1. Functional Symbol and Typical Application

#### Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Storage Temperature Range	-65 to +150	°C

Table 4. D.C. OPERATING CHARACTERISTICS (Vcc = 1.7 V to 5.5 V, Ta = -40 to +125°C, unless oth	herwise specified)
---	--------------------

Symbol	Parameter	Test Conditions	Min	Max	Units
I <sub>CCR</sub>	Read Current	Read, f <sub>SCL</sub> = 400 kHz/1 MHz		1	mA
I <sub>CCW</sub>	Write Current			2.5	mA
I <sub>SB</sub>	Standby Current				

		Stan	dard	Fa	st	Fast	Plus	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
F <sub>SCL</sub>	Clock Frequency		100		400		1,000	kHz
t <sub>HD:STA</sub>	START Condition Hold Time	4		0.6		0.26		μs
t <sub>LOW</sub>	Low Period of SCL Clock	4.7		1.3		0.50		μs
t <sub>HIGH</sub>	High Period of SCL Clock	4		0.6		0.26		μs
t <sub>SU:STA</sub>	START Condition Setup Time	4.7		0.6		0.26		μs
t <sub>HD:DAT</sub>	Data In Hold Time	0		0		0		μs
t <sub>SU:DAT</sub>	Data In Setup Time	250		100		50		ns
t <sub>R</sub> (Note 7)	SDA and SCL Rise Time		1,000	20	300		100	ns
t <sub>F</sub> (Note 7)	SDA and SCL Fall Time		300	20	300		100	ns
t <sub>SU:STO</sub>	STOP Condition Setup Time	4		0.6		0.25		μs
<sup>t</sup> BUF	Bus Free Time Between STOP and START	4.7		1.3		0.5		μs
t <sub>AA</sub>	SCL Low to Data Out Valid		3.5		0.9		0.45	μs
t <sub>DH</sub>	Data Out Hold Time	100		100		50		ns

#### Table 6. A.C. CHARACTERISTICS (Note 6)

T<sub>i</sub> (Note 7)

Noise Pulse Filtet1lse Filtet1liat 9.754 6 6.5 91.6724 4\*929 iSDC171 refBT8 088m8 088m8 0y

#### Power On Reset (POR)

The N24C256X incorporates Power On Reset (POR) circuitry which protects the device against powering up in the wrong state.

The N24C256X will power up into Standby mode after V<sub>CC</sub> exceeds the POR trigger level and will power down into Reset mode when V<sub>CC</sub> drops below the POR trigger level. This bi directional POR feature protects the device against 'brown out' failure following a temporary loss of power.

#### **Pin Description**

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master.

SDA:



Figure 3. Start/Stop Conditions

DEVICE ADDRESS

								`
Memory Array Access	1	0	1	0	0	0	1	R/W
UID, Device Config.	1	0	1	1	0	0	1	R/W

Figure 4. Slave Address Bits







#### Figure 6. Bus Timing

	П

#### **READ OPERATIONS**

#### Immediate Read

Upon receiving a Slave address with the R/W bit set to '1', the N24C256X will interpret this as a request for data residing at the current byte address in memory. The N24C256X will acknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the N24C256X returns to Standby mode.

#### Selective Read

To read data residing at a specific location, the internal address counter must first be initialized as described under Byte Write. If rather than following up the two address bytes with data, the Master instead follows up with an Immediate Read sequence, then the N24C256X will use the 15 active address bits to initialize the internal address counter and will shift out data residing at the corresponding location. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 11), the N24C256X returns to Standby mode.

#### Sequential Read

If during a Read session the Master acknowledges the 1<sup>st</sup> data byte, then the N24C256X will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 12). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap around at end of memory (rather than end of page).

#### **Device Configuration Register Read**

The Device Configuration Register Read instruction is similar to a Selective Read instruction. The user must send the device header and the two address bytes as for a Device Configuration Register Write instruction. This dummy write instruction is followed by an Immediate Read with the device header 1011b, and the device will shift back the content of the Device Configuration Register. Don't care bits are read as 1s.

If the master acknowledges the data byte, requesting more data, the device will continue to return the content of the Device Configuration Register until the Master responds with a NoACK.

#### Unique ID Number Read

The Unique ID Number Read instruction is similar to a Sequential Read instruction. The user must send the device header starting with 1011b followed by the 001 bits. As specified in Table 8, the second byte consists of xxxx x01x and the third byte if xxxx 0000, where x is don't care. This dummy write instruction is followed by an Immediate Read with the device header 1011b, and the device will shift back the Unique ID byte by byte. The Unique ID is 16 bytes (128 bits) long. The first byte contains the manufacturer ID and the second byte contains the device ID (Figure 13). After the last byte of the Unique ID has been shifted, if the master acknowledges (requesting more data), the device will wrap around and start returning the Unique ID from the beginning.

#### **Delivery State**

The N24C256X is shipped erased, i.e., all memory array bytes are FFh and the settable Device Configuration SWP bit set to 0 (3Dh).



Figure 10. Immediate Read Sequence and Timing



