256 kb L P e Se ial SRAM

32 k x 8 Bit Organization

Introduction

The ON Semiconductor serial SRAM family includes several integrated memory devices including this 256 kb serially accessed Static Random Access Memory, internally organized as 32 k words by 8 bits. The devices are designed and fabricated using ON Semiconductor's advanced CMOS technology to provide both high speed performance and low power. The devices operate with a single chip select ($\overline{\text{CS}}$) input and use a simple Serial Peripheral Interface (SPI) serial bus. A single data in and data out line is used

along 4.8448₽.46 0 TD1:002 Tcvices opodes ss d itemices ure rangopof (high)T/TT5 610 425.3509 0 TD 0 TD@0ef ₮/TT6 1578₽.46 0 TD1:

Table 6. TIMING TEST CONDITIONS

Item			
Input Pulse Level	0.1 V _{CC} to 0.9 V _{CC}		
Input Rise and Fall Time	5 ns		
Input and Output Timing Reference Levels	0.5 V _{CC}		
Output Load	CL = 100 pF		
Operating Temperature	−40 to +85°C		

Table 7. TIMING

Item	Symbol	Min	Max	Units
Clock Frequency	f _{CLK}		16	MHz
Clock Rise Time	•	•	•	

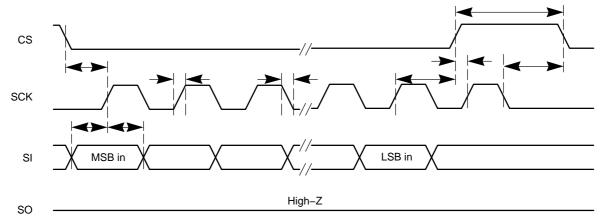
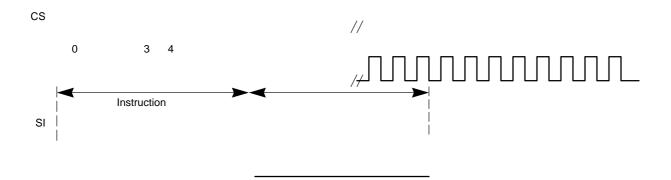


Figure 3. Serial Input Timing



8. CONTROL SIGNAL DESCRIPTIONS				



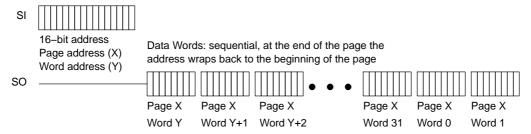


Figure 8. Page READ Sequence

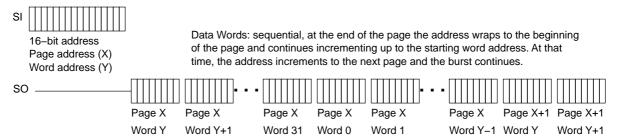


Figure 9. Burst READ Sequence

WRITE Operations

The serial SRAM WRITE is selected by enabling $\overline{\text{CS}}$ low. First, the 8 bit WRITE instruction is transmitted to the device followed by the 16 bit address with the MSB being a don't care. After the WRITE instruction and addresses are sent, the data to be stored in memory is shifted in on the SI pin.

If operating in page mode, after the initial word of data is shifted in, additional data words can be written as long as the address requested is sequential on the same page. Simply write the data on SI pin and continue to provide clock pulses. The internal address pointer is automatically incremented to the next higher address on the page after each word of data is written in. This can be continued for the entire page length of 32 words long. At the end of the page, the addresses pointer will be wrapped to the 0 word address within the

page and the operation can be continuously looped over the 32 words of the same page. The new data will replace data already stored in the memory locations.

If operating in burst mode, after the initial word of data is shifted in, additional data words can be written to the next sequential memory locations by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each word of data is read out. This can be continued for the entire array and when the highest address is reached (7FFFh), the address counter wraps to the address 0000h. This allows the burst write cycle to be continued indefinitely. Again, the new data will replace data already stored in the memory locations.

All WRITE operations are terminated by pulling \overline{CS} high.

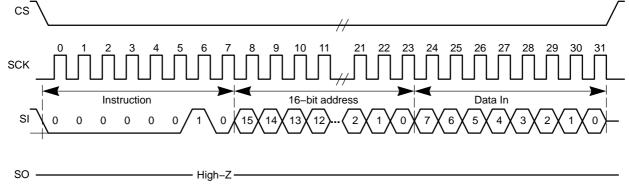
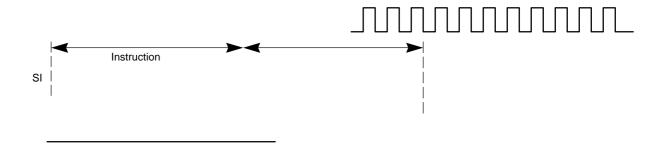


Figure 10. Word WRITE Sequence

cs



WRITE Status Register Instruction (WRSR)

This instruction provides the ability to write the status register and select among several operating modes. Several of the register bits must be set to a low '0' if any of the other

bits are written. The timing sequence to write to the status register is shown below, followed by the organization of the status register.

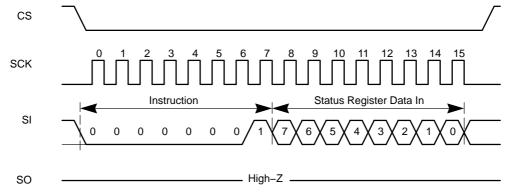


Figure 14. WRITE Status Register Sequence

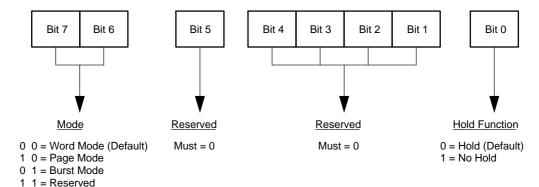
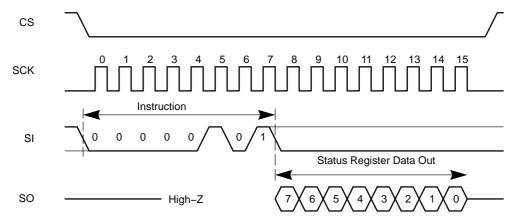


Figure 15. Status Register

READ Status Register Instruction (RDSR)

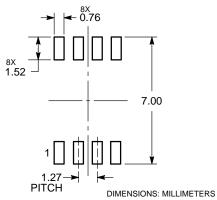
This instruction provides the ability to read the Status register. The register may be read at any time by performing the following timing sequence.





DATE 18 MAY 2015

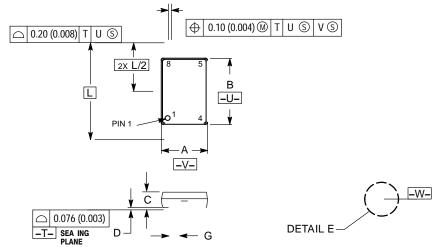
RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

TSSOP-8 3.0x4.4x1.1 CASE 948S ISSUE C

DATE 20 JUN 2008



- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- PROTRUSIONS SHALL NOT EXCEED 0.25 (0.010)
 PER SIDE.

 5. TERMINAL NUMBERS ARE SHOWN FOR
 REFERENCE ONLY.
 6. DIMENSION A AND B ARE TO BE DETERMINED
 AT DATUM PLANE -W-.

	MILLIME ERS		INCHES	
DIM	MIN	MA	MIN	MA
Α	2.90	3.10	0.114	0.122
В	4.30	4.50	0.169	0.177
С		1.10		0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026	BSC

L	6.40 BSC		0.252 BSC		
M	0°	8°	0°	8°	l

GENERIC MARKING DIAGRAM*



