N64S830HA

64 kb Low Power Serial SRAM

8 k x 8 Bit Organization

ON Semiconductor

http://onsemi.com

Introduction

The ON Semiconductor serial SRAM family includes several integrated memory devices including this 64 k serially accessed Static Random Access Memory, internally organized as 8 k words by 8 bits. The devices are designed and fabricated using ON Semiconductor's advanced CMOS technology to provide both high speed performance and low power. The devices operate with a single chip select ($\overline{CS}$) input and use a simple Serial Peripheral Interface (SPI) serial bus. A single data in and data out line is used along with a clock to access data within the devices. The N64S830HA devices include a $\overline{HOLD}$ pin that allows communication to the device to be paused. While paused, input transitions will be ignored. The devices can operate over a wide temperature range of 40°C to +85°C and can be available in several standard package offerings.

Features

- **Power Supply Range:** 2.5 to 3.6 V
- **Very Low Standby Current:** As low as 1 μA
- **Very Low Operating Current:** As low as 3 mA
- **Simple Memory Control:**
  Single chip select ($\overline{CS}$)
  Serial input (SI) and serial output (SO)
- **Flexible Operating Modes:**
  Word read and write
  Page mode (32 word page)
  Burst mode (full array)
- **Organization:** 8 k x 8 bit
- **Self Timed Write Cycles**
- **Built−in Write Protection ($\overline{CS}$ High)**
- **$\overline{HOLD}$ Pin for Pausing Communication**
- **High Reliability:** Unlimited write cycles
- Green SOIC and TSSOP
- These Devices are Pb Free, Halogen Free/BFR Free and are RoHS Compliant

ORDERING INFORMATION

Device	Package	Shipping†
N64S830HAS22I	SOIC−8 (Pb−Free)	100 Units / Tube
N64S830HAT22I	TSSOP−8 (Pb−Free)	100 Units / Tube
N64S830HAS22IT	SOIC−8 (Pb−Free)	3000 / Tape & Reel
N64S830HAT22IT	TSSOP−8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification

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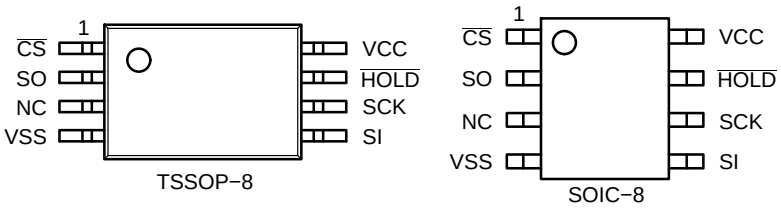


Figure 1. Pin Connections
(Top View)

Table 1. DEVICE OPTIONS

Part Number	Density	Power Supply (V)	Speed (MHz)	Package	Typical Standby Current	Read/Write Operating Current
N64S830HAS2	64 Kb	3.0	20	SOIC	1 μA	3 mA @ 1 Mhz
N64S830HAT2				TSSOP		

Table 2. PIN NAMES

Pin Name	Pin Function
$\overline{CS}$	Chip Select Input
SCK	Serial Clock Input
SI	Serial Data Input
SO	Serial Data Output
$\overline{HOLD}$	Hold Input
NC	No Connect
V_{CC}	Power
V_{SS}	Ground

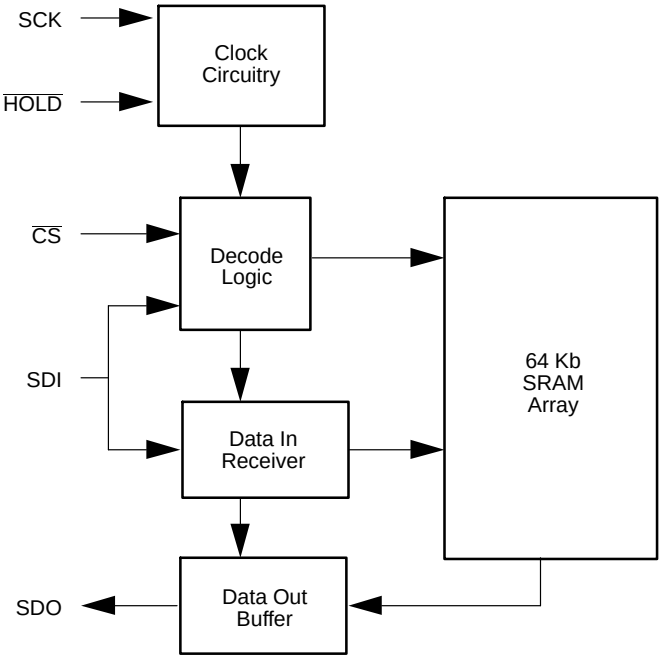
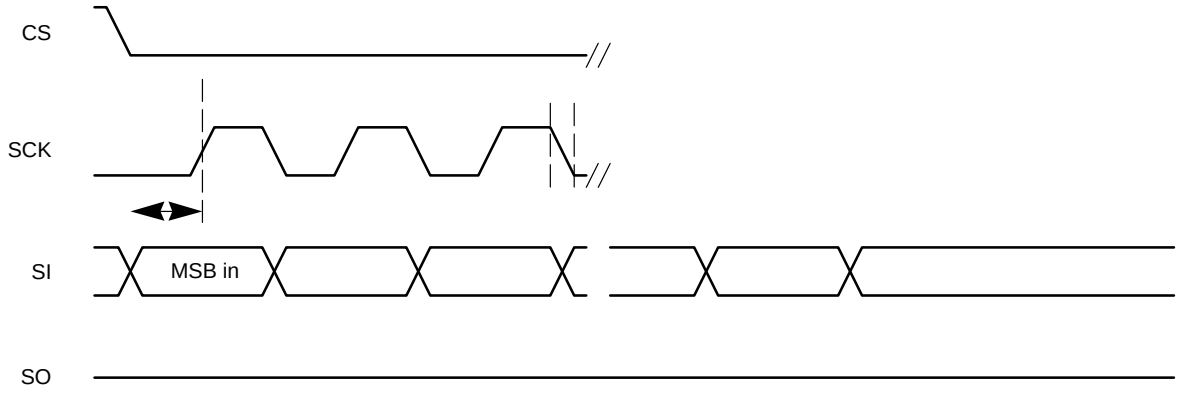
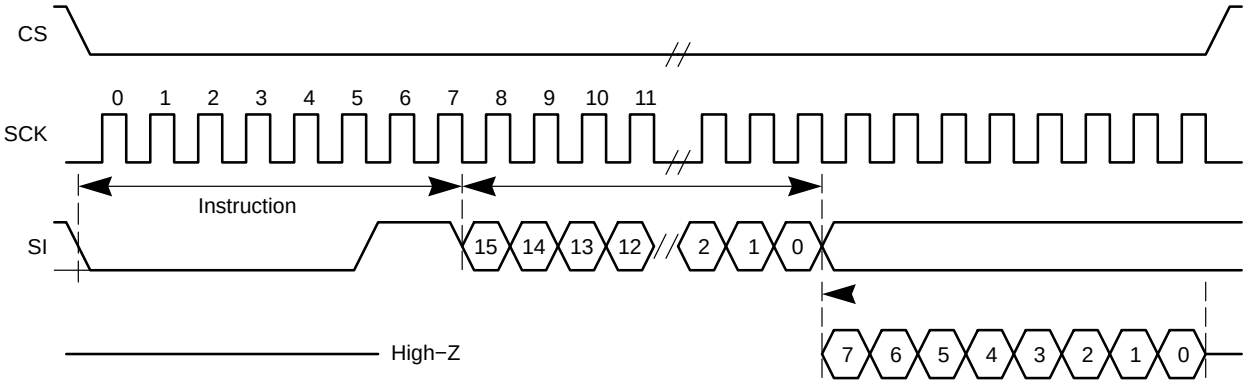


Figure 2. Functional Block Diagram

Table 3. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC} + 0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to 125	°C


CS
SCK
SI
MSB in
SO


CS
SCK
0 1 2 3 4 5 6 7 8 9 10 11
Instruction
SI
15 14 13 12 2 1 0
High−Z
7 6 5 4 3 2 1 0

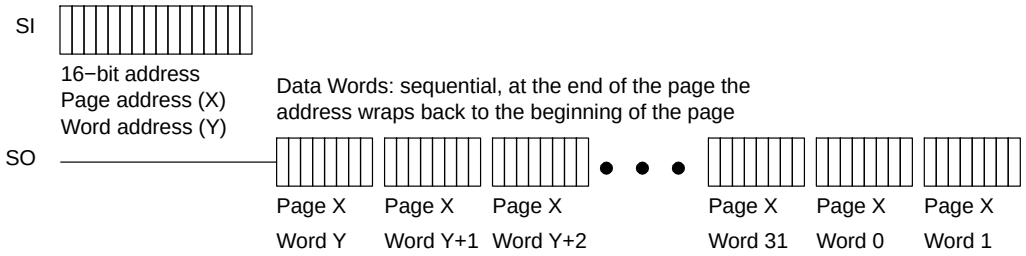


Figure 8. Page READ Sequence

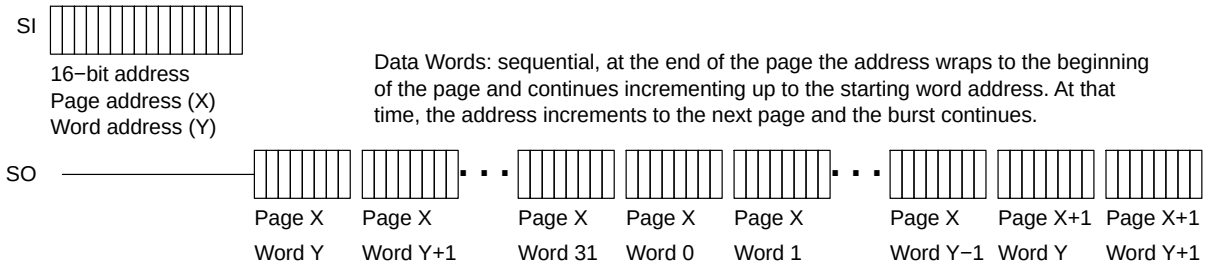


Figure 9. Burst READ Sequence

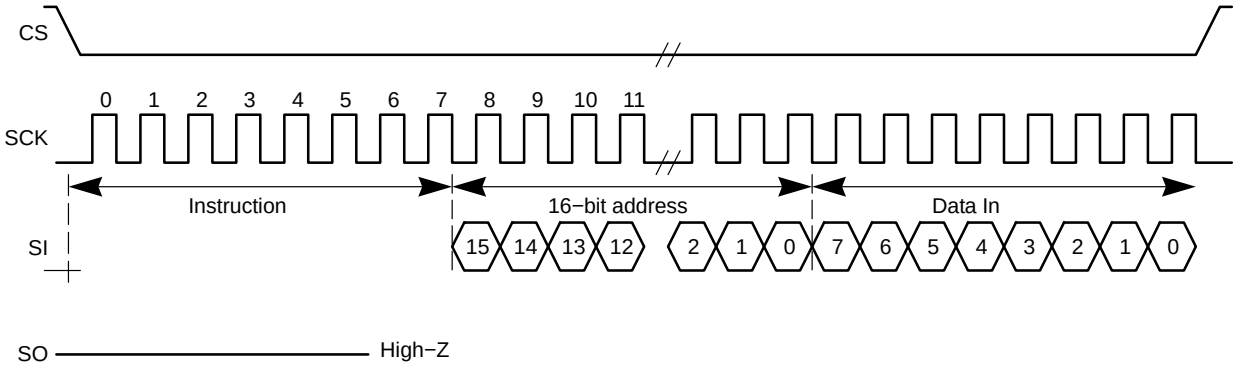
WRITE Operations

The serial SRAM WRITE is selected by enabling $\overline{CS}$ low. First, the 8 bit WRITE instruction is transmitted to the device followed by the 16 bit address with the 3 MSBs being don't care. After the WRITE instruction and addresses are sent, the data to be stored in memory is shifted in on the SI pin.

If operating in page mode, after the initial word of data is shifted in, additional data words can be written as long as the address requested is sequential on the same page. Simply write the data on SI pin and continue to provide clock pulses. The internal address pointer is automatically incremented to the next higher address on the page after each word of data is written in. This can be continued for the entire page length of 32 words long. At the end of the page, the addresses pointer will be wrapped to the 0 word address within the page and the operation can be continuously looped over the 32 words of the same page. The new data will replace data already stored in the memory locations.

If operating in burst mode, after the initial word of data is shifted in, additional data words can be written to the next sequential memory locations by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each word of data is read out. This can be continued for the entire array and when the highest address is reached (1FFFh), the address counter wraps to the address 0000h. This allows the burst write cycle to be continued indefinitely. Again, the new data will replace data already stored in the memory locations.

All WRITE operations are terminated by pulling $\overline{CS}$ high.



WRITE Status Register Instruction (WRSR)

This instruction provides the ability to write the status register and select among several operating modes. Several of the register bits must be set to a low ‘0’. The timing sequence to write to the status register is shown below, followed by the organization of the status register.

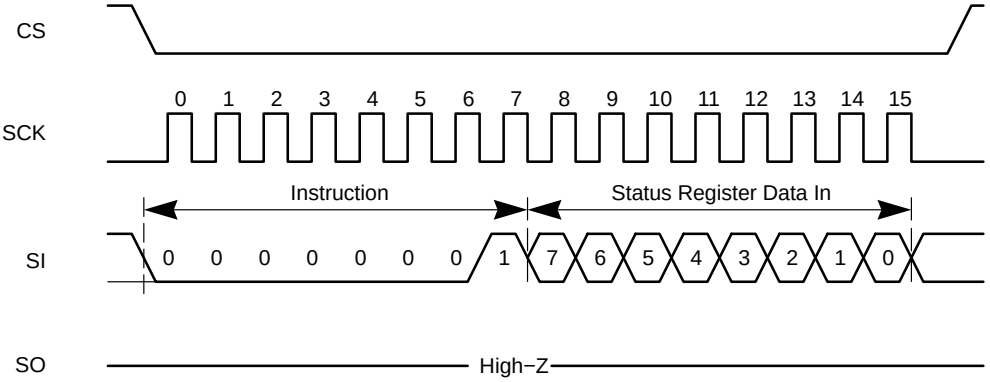


Figure 14. WRITE Status Register Sequence

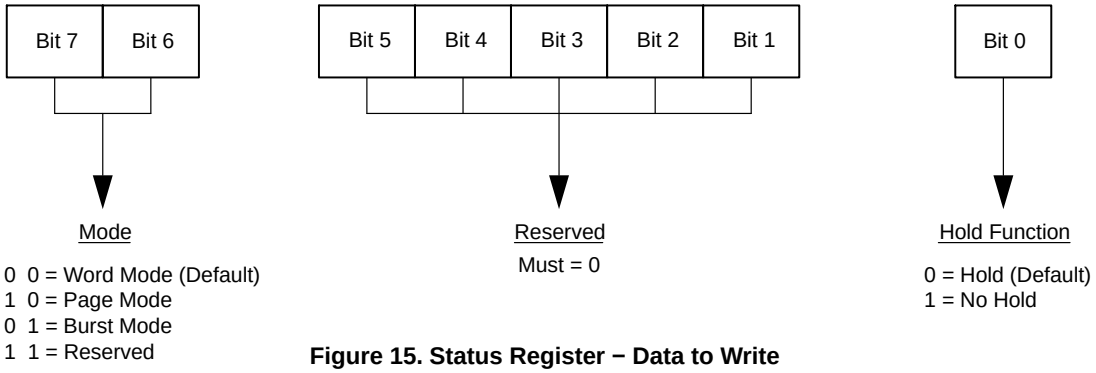


Figure 15. Status Register − Data to Write

READ Status Register Instruction (RDSR)

This instruction provides the ability to read the programmable bits of the Status R

SCALE 1:1

SOIC 8

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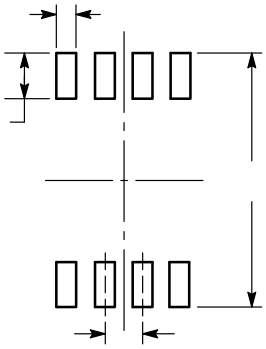
SOLDERING FOOTPRINT*



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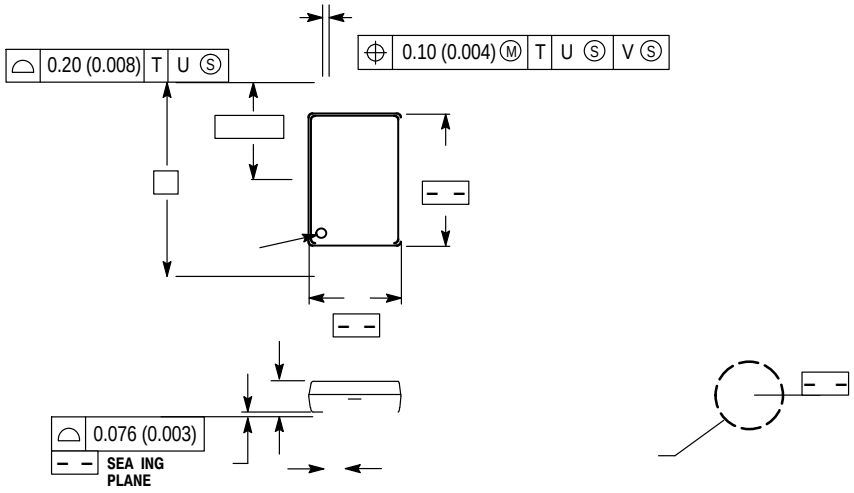
CASE 948S
ISSUE C

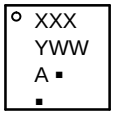
DATE 20 JUN 2008



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIME ERS		INCHES	
DIM	MIN	MA	MIN	MA
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	

L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



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