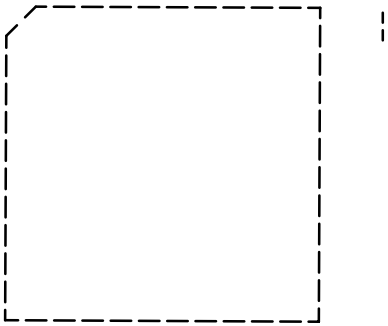


3,9,18,19,20	V _{CC}			Positive Supply Voltage. All VCC Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
15,24	V _{EE}			Negative Supply Voltage. All VEE Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
6,12	V _{BB0}			

			—	—
X	X	H	a	a
L	L	L	b	b
L	H	L	b	a
H	H	L	a	a
H	L	L	a	b



$\overline{D0b}$

V_{CC}	Positive Mode Power Supply	$V_{EE} = 0\text{ V}$		6	V
V_{EE}	Negative Mode Power Supply	$V_{CC} = 0\text{ V}$		6	V
V_I	Positive Mode Input Voltage Negative Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			40 to +85	$^{\circ}\text{C}$
T_{stg}	Storage Temperature Range			65 to +150	$^{\circ}\text{C}$
θ_{JA}	Thermal Resistance (Junction to				

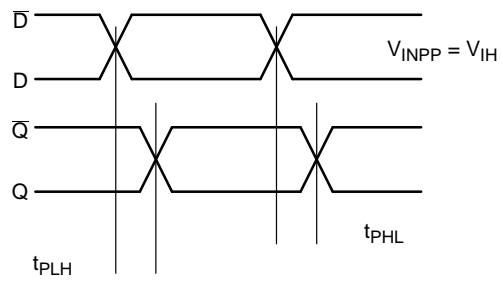
$V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Not

		- °	
I_{EE}	Negative Power Supply Current	35	45
V_{OH}	Output HIGH Voltage (Note 7)	2155	2280
V_{OL}	Output LOW Voltage (Note 7)	1355	1575
V_{IH}	Input HIGH Voltage (SEL0, SEL1, COM_SEL) Input HIGH Voltage (D Inputs)	2135 2135	
V_{IL}	Input LOW Voltage (SEL0, SEL1, COM_SEL) Input LOW Voltage (D Inputs)	V_{EE} 1355	
V_{BB}	Output Reference Voltage (Note 8)	1775	1875
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9)	1.2	
I_{IH}	Input HIGH Current (@ V_{IH})		
I_{IL}	Input LOW Current (@ V_{IL})	D \bar{D} SEL	0.5 150 150

V_{CC} = 0 V; V_{EE} = 2.375 V to 3.8 V or V_{CC} = 2.375 V to 3.8 V; V_{EE} = 0 V (Note 14)

		-			°			°																																																									
V _{OUTPP}	Output Voltage Amplitude (See Figure 3)	f _{in} ≤ 1 GHz 525	f _{in} ≤ 2 GHz 500	f _{in} = 2.5 GHz 400	700	600	500	550	700	600	500	700	500	400	300	mV																																																	
t _{PLH} , t _{PHL}	Propagation Delay to Output Differential D to Q, \bar{Q} SEL to Q, \bar{Q} COM_SEL to Q, \bar{Q}	375	500	625	400	525	650	450	575	700	375	500	625	400	525	650	450	575	700	1100	1100	ps																																											
t _{Skew}	Pulse Skew (Note 15) Within Device Input Skew (Note 16) Within Device Output Skew (Note 17) Device to Device Skew (Note 18)		10	50		10			10	50		10	50		10	50		10	50	200	200	ps																																											
t _{JITTER}	RMS Random Clock Jitter (Note 19) @ ≤ 1.0 GHz @ ≤ 1.5 GHz @ ≤ 2.0 GHz @ ≤ 2.5 GHz Peak to Peak Data Dependent Jitter (Note 20) @ 0.5 GHz @ 1.25 GHz @ 2.488 GHz		0.269	0.4		0.307	0.4		0.371	0.5		0.306	0.4		0.303	0.4		0.391	0.6		0.250	0.4		0.305	0.5		0.722	1.2		0.339	0.8		0.895	2.0		2.443	7.7		4.1	16		4.6	15		4.4	16		32.2	80		22.6	63		22	53		30.8	66		27.2	56		24.4	54	ps

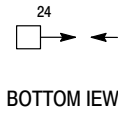
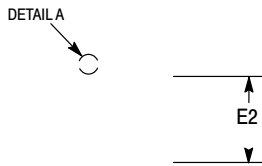
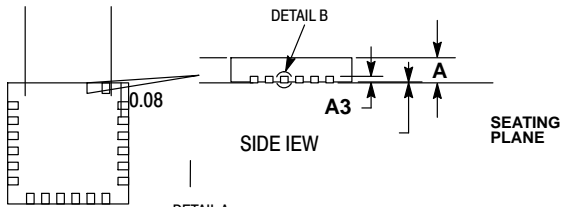
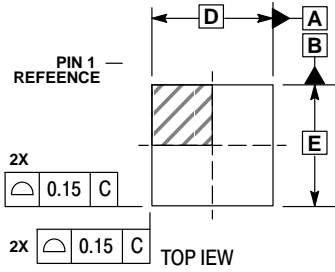
V_{INPP}



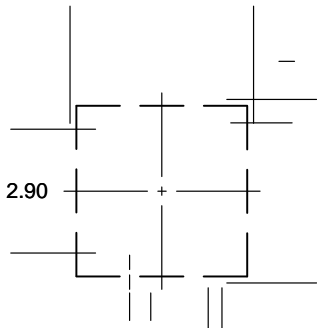
QFN24, 4x4, 0.5P
CASE 485L
ISSUE B

DATE 05 JUN 2012

f2.836
 0.41 cm 0 0
SCALE 2:1



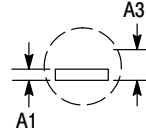
SOLDERING FOOTPRINT



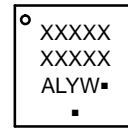
DIMENSIONS: MILLIMETERS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

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