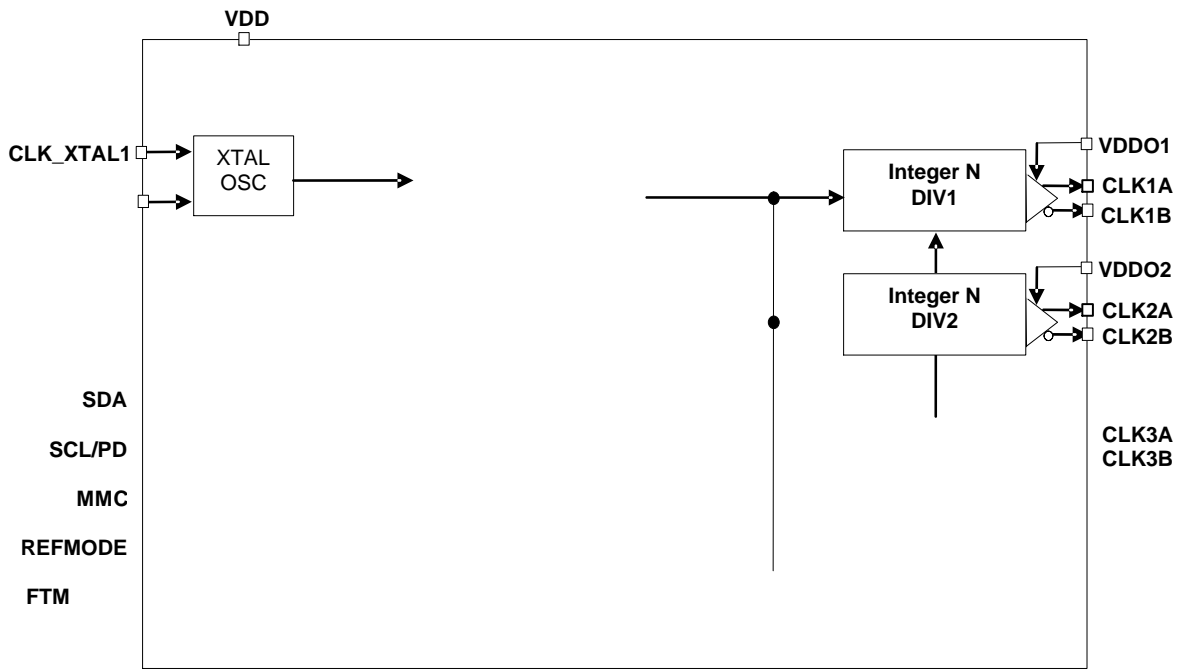


2.5 V / 3.3 V Low Noise Multi-Rate Clock Generator

NB3H5150-01

Description

NB3H5150-01





NB3H5150-01

Table 1. PIN DESCRIPTION

| Pin | Name | I/O | Description |
|-----|-------------|---|--|
| 32 | CLK_XTAL1 | Crystal or LVTTTL/LVCMOS or LVPECL/LVDS Input | Crystal Input or Single-Ended or Differential Clock Input; If CLK_XTAL1 is used as single-ended input, CLK_XTAL2 must be connected to ground. See Table 2. |
| EP | Exposed Pad | Ground | Ground – Negative Power Supply is connected via the Exposed Pad . The Exposed Pad (EP) on the QFN-32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat sinking conduit. The pad is electrically connected to the die, carries all power supply return currents and must be electrically connected to GND. |

1. All VDD, AVDDn, VDDOn, EP (GND) pins must be externally connected to a power supply for proper operation. VDD and AVDDn must all be at the same voltage.

NB3H5150-01 BASIC OPERATION

Introduction

NB3H5150-01

become effective and will begin to output the selected frequencies.

- Subsequent changes to any FS pin(s) will cause the associated CLK(n) output(s) to momentarily go to static levels, and then to resume at the new frequency; CLK(n) will follow the FS(n) pin programmable Tables 3 and 4 for output frequencies and interface levels.

Note that in changing from LVPECL to LVCMOS (or vice-versa), output logic levels cannot be guaranteed. This is because the receiver inputs are not likely to change in a given application, and the LVPECL output loading in the application will also not change. It is logical to presume that the output type will be predetermined and fixed.

Therefore, in a system/application, the user should

be aware that subsequent change to the FS pin should only change frequency, and not output type.

- Power off/on cycle will repeat the entire sequence
- Power Down**

To initiate the Power-Down mode, the SDA pin must be LOW and remain LOW. If the SCL/PD pin is taken HIGH at any time, the device enters a complete power-down mode with a current consumption of less than 1 mA for the entire device. When SCL/PD is subsequently taken LOW, the device will function as though power were removed and re-applied. That is, sequencing will begin at #1.

Power-down is also available via I²C with a register file.

FS(n) Pin Programmable Selection of Output Frequencies and Levels

Table 3. NB3H5150-01MNTXG – CLK1A:3A & CLK1B:3B OUTPUT FREQUENCY SELECT TABLE WITH 25 MHz CRYSTAL

| Logic Level | FS1 (CLK1) (MHz) | FS2 (CLK2) (MHz) | FS3 (CLK3) (MHz) |
|---------------------|-----------------------|------------------------|------------------------|
| Low | 156.25 (LVPECL) | 156.25 (LVPECL) | 156.25 (LVPECL) |
| Mid / Float* | 25.00 (LVPECL) | 100.00 (LVPECL) | 125.00 (LVPECL) |
| High | 50.00 (LVPECL) | 125.00 (LVPECL) | 50.00 (LVPECL) |

*(Default)

Table 4. NB3H5150-01MNTXG – CLK4A & CLK4B OUTPUT FREQUENCY SELECT TRUTH TABLE (MHz) WITH 25 MHz CRYSTAL*

| FS4A | FS4B | CLK4 (MHz) | Divider Type |
|---------------------|---------------------|------------------------|----------------|
| Low | Low | 33.33 (LVCMOS) | Integer |
| Low | Mid / Float | 66.66 (LVCMOS) | Fractional |
| Low | High | 133.33 (LVCMOS) | Fractional |
| Mid / Float | Low | 133.33 (LVPECL) | Fractional |
| Mid / Float* | Mid / Float* | 156.25 (LVPECL) | Integer |
| Mid / Float | High | 125.00 (LVPECL) | Integer |
| High | Low | 25.00 (LVPECL) | Integer |
| High | Mid / Float | 100.00 (LVPECL) | Integer |
| High | High | 161.1328 (LVPECL) | Fractional |

*(Default)

I²C MODE: (see Table 5)

Some features that are not available in pin-strap mode can be obtained in I²C mode, such as Output Enable/Disable, By-Pass mode and Power-Down. In addition, output frequency and output levels can also be I²C controlled.

The NB3H5150-01 I²C Programming Guide can be found on the NB3H5150-01 web site. This application note provides details on configuring the NB3H5150-01 by writing to registers in the NB3H5150-01 with approved register files through the I²C/SMBus interface.

<http://www.onsemi.com/pub/Collateral/NB3H5150-01%20I2C%20PROGRAMMING%20GUIDE%20%20..PDF>

Register Files can be generated by the factory upon request.

Prerequisites:

- SDA and SCL must be connected to I²C SMBus
- SDA must be logic High.
 1. Upon device power-up.
 - A All four frequencies and output type selections will be preloaded according to the FS_n pin settings, but all four outputs will be held at static LVPECL levels until the PLL has become stable.
NOTE: After power up, changes to FS pins will be blocked from controlling device operation.
 - B Once the PLL is stable, the Mixed Mode Control pin (MMC) is checked:
 - i. If MMC is LOW, all CLK(n) outputs will remain at static LVPECL levels.
 - ii. If MMC is HIGH and FS4A is LOW, CLK1, CLK2, and CLK3 outputs will remain at static LVPECL levels.
CLK4A/4B output frequency and output levels will become active after PLL stabilization time according to FS4A and FS4B pin selection in Table 4.
After power up, changes to all pins will be ignored.
 - iii. If MMC is HIGH and FS4A MID or HIGH, CLK1, CLK2, and CLK3 output frequency and type will become active after PLL stabilization time according to their respective FS1, FS2 and FS3 pin selection in Table 3.

CLK4A/4B outputs remain at Static LVPECL Levels.

After power up, changes to all pins will be ignored except the SDA and SCL inputs.

iv. The FS4A and FS4B pins set the bus address when MMC pin is LOW (see Table 5, I²C Device Address Table).

C The I²C interface can now be used to load register files into the NB3H5150-01. In I²C Mode, configuration of Output Enables, output frequency, output levels of each output, specific block power-down control, bypass mode, etc. are all possible.

D Any outputs which were held in static level mode (described above) will be released for operation.

CLK(n) outputs will be active at the programmed frequencies and levels.

CLK(n) outputs will react to any subsequent changes to thhangel

Table 5. SDA, SCL AND MMC CONTROL PINS FOR OUTPUT FUNCTION

| Mode | SDA | SCL/PD | MMC | Comments | Outputs (Note 2) | |
|------------|-------------|-------------|-----------------------|----------|----------------------------|----------------------------|
| | | | | | CLK1, CLK2, CLK3 | CLK4 |
| Mixed Mode | H Note 4 | H Note 4 | L | | Static LVPECL Logic Levels | Static LVPECL Logic Levels |
| | H Note 4 | H Note 4 | H FS4A = L | | Static LVPECL Logic Levels | Active per Table 4 |
| | H Note 4 | H Note 4 | H FS4A = M or H | | Active per Table 3 | Static LVPECL Logic Levels |

2. All outputs are static until after the PLL is stable.
 3. Any changes to the device configuration after power-up are made by reading and writing to registers through the I2C interface.
 4. Don't care state unless device address is matched by controller address.
- X = don't care

Table 6. ATTRIBUTES

| Characteristics | | Value |
|--|--|------------------------------|
| ESD Protection | Human Body Model Machine Model Charge Device Model | > 2 kV > 150 V > 500 V |
| Moisture Sensitivity (Note 5) | 32-QFN | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | | 245, 894 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

Table 7. MAXIMUM RATINGS

| Symbol | Parameter | Condition | Rating | Unit |
|-------------------|---|------------------|---------------------------------|--------------|
| V _{DD} | Positive Power Supply – Core | GND = 0 V | 3.63 | V |
| AV _{DDn} | Positive Power Supply – Analog | GND = 0 V | 3.63 | V |
| V _{DDOn} | Positive Power Supply – Outputs | GND = 0 V | 3.63 | V |
| V _{IO} | Positive Input/Output Voltage | GND = 0 V | -0.5 to V _{DD} +0.5 | V |
| V _I | Positive Input Voltage SDA and SCL | GND = 0 V | 5.5 | V |
| T _A | Operating Temperature Range | QFN-32 | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | -65 to +150 | °C |
| θ _J | Maximum Junction Temperature | | 125 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) (Note 6) | QFN-32 QFN-32 | 0 lfpm 500 lfpm | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) (Note 6) | QFN-32 | | °C/W |
| T _J | Maximum Junction Temperature | | 125 | °C |
| T _{sol} | Wave Solder Pb-Free, 10 sec | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

6. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 8. DC CHARACTERISTICS

V_{DD} = AV_{DDn} = 3.3 V ±5% or 2.5 V ±5%; V_{DDOn} = 3.3 V ±5% or 2.5 V ±5% or 1.8 V ±5%; GND = 0 V; T_A = -40°C to 85°C

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|--------------------------------|--|------|
| POWER SUPPLY / CURRENT (Note 12) | | | | | |
| V _{DD} /AV _{DDn} | Core Power Supply | V _{DD} = AV _{DDn} = 3.3 V 2.375 | 3.3 2.5 | 3.465 2.625 | V |
| V _{DDOn} | Output Power Supply | V _{DDOn} = 3.3 V 2.375 V _{DDOn} = 2.5 V 1.71 | 3.3 2.5 1.8 | 3.465 2.625 1.89 | |
| I _{DD} /I _{ADDn} | Core and Input Power Supply Current for V _{DD} and AV _{DDn} V _{DD} = 3.3 V CLK4 Integer CLK4 Frac-N V _{DD} = 2.5 V CLK4 Integer CLK4 Frac-N | | 60 75 55 70 | 75 90 70 85 | mA |
| I _{DDOn} | Output Buffer Power Supply Current for V _{DDOn} Incremental I _{DDO} Current by One Output Bank and Output Type LVPECL – One differential LVPECL output pair (CLKnA & CLKnB) Frequency Independent V _{DDO} = 3.3 V V _{DDO} = 2.5 V LVCMOS – Two LVCMOS outputs (CLKnA & CLKnB) V _{DDO} = 3.3 V V _{DDO} = 2.5 V V _{DDO} = 1.8 V | | 40 40 20 17 15 | 50 50 25 25c(DDO)Tj8 0 0 8 5071 re 9 TD(7 | |

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Table 9. AC CHARACTERISTICS

$V_{DD} = AV_{DDn} = 3.3\text{ V} \pm 5\%$ or $2.5\text{ V} \pm 5\%$; $V_{DDO} = 3.3\text{ V} \pm 5\%$ or $2.5\text{ V} \pm 5\%$ or $1.8\text{ V} \pm 5\%$; $GND = 0\text{ V}$; $T_A = -40^\circ\text{C}$ to 85°C (Note 13)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|-----------------|--|--------------------|--|--|---------------|
| f_{CLKIN} | External Clock / Crystal Input Frequency – PLL Mode | -1000 ppm | 25 | +1000 ppm | MHz |
| f_{INBP} | External Clock Input Frequency – PLL Bypass Mode I ² C Mode; $f_{in} = f_{out}$ | 1 | | 50 | MHz |
| $f_{CLK1,2,3}$ | CLK1, CLK2, CLK3 Typical Output Clock Frequencies; $f_{in} = 25\text{ MHz}$ | | 25 50 100 125 156.25 | | MHz |
| f_{CLK4} | CLK4 Outputs Typical Output Clock Frequencies; $f_{in} = 25\text{ MHz}$ Resolution of 1 Hz Integer Frac-N | | 25 33.33 100 125 156.25 66.66 133.33 161.1328 | | MHz |
| $f_{SDA/SCL}$ | Serial Data and Clock Rates | | 100k | | bps |
| t_{PWsCL} | Serial Clock Pulse Width | 1 | | | μs |
| t_{Wt} | Time SCL/PD Pin must be Held Low to “Wake-up” the Device | 100 | | | ns |
| t_{DC} | Output Clock Duty Cycle (Crystal or Reference Duty Cycle = 50%) PLL Mode; $<1\text{ ns } t_f / t_r$ LVPECL $f_{out} = 156.25\text{ MHz}$ LVCMOS $f_{out} = 33.33\text{ MHz}$ PLL Bypass Mode; Input Duty Cycle = 50%, $V_{INPP} \geq 1.2\text{ V}$ | 47.5 47.5 45 | 50 50 | 52.5 52.5 55 | % |
| Φ_N | Phase Noise (Integer-N) $f_{out} = 156.25\text{ MHz}$, $f_{in} = 25\text{ MHz}$ Crystal, LVPECL | | 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz | -115 -130 -140 -145 -153 -153 | dBc |
| Φ_N | Phase Noise (Integer-N) $f_{out} = 100\text{ MHz}$, $f_{in} = 25\text{ MHz}$ Crystal, LVCMOS | | 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz | -120 -136 -142 -145 -156 -156 | dBc |
| Φ_N | Phase Noise (Frac-N) $f_{out} = 161.1328\text{ MHz}$, $f_{in} = 25\text{ MHz}$ Crystal, LVPECL | | 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz | -118 -128 -130 -132 -153 -153 | dBc |
| Φ_N | Phase Noise (Frac-N) $f_{out} = 133.33\text{ MHz}$, $f_{in} = 25\text{ MHz}$ Crystal, LVCMOS | | 1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz | -117 -126 -126 -131 -153 -153 | dBc |
| $t_{jit}(\Phi)$ | RMS Phase Jitter – 25 MHz Crystal (Note 15) Integration Range: 12 kHz – 20 MHz $f_{out} = 156.25\text{ MHz}$, Integer CLK _n $f_{out} = 161.1328\text{ MHz}$; Frac-N CLK4 | | | 300 1000 | fs |

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Table 9. AC CHARACTERISTICS

$V_{DD} = AV_{DDn} = 3.3\text{ V} \pm 5\%$ or $2.5\text{ V} \pm 5\%$; $V_{DDO} = 3.3\text{V} \pm 5\%$ or $2.5\text{ V} \pm 5\%$ or $1.8\text{ V} \pm 5\%$; $GND = 0\text{ V}$; $T_A = -40^\circ\text{C}$ to 85°C (Note 13)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|--------------------------------|---|------------|------------------|-------------|------|
| tjit(Φ) | Additive RMS Phase Jitter (PLL Bypass in I ² C Mode) Integration Range:12 kHz – 5 MHz f _{out} = 25 MHz, CLK1 LVCMOS | | 50 | | fs |
| tpd | Input to Output Propagation Delay (PLL Bypass in I ² C Mode) 25 MHz | | 5 | | ns |
| PSRR | Ripple Induced Phase Spur Level 100 kHz & 1 MHz, 100 mV _{pp} , Ripple Injected on V _{DD} /AV _{DDn} ≤ 100 MHz | | -60 | | dBc |
| t _r /t _f | Output Rise/Fall Times (CLKnA/CLKnB), 20% – 80% of VDDO _n f _{out} = 156.25 MHz LVPECL f _{out} = 33.33 MHz @ VDDO = 3.3 V LVCMOS – 5 pF | 120 500 | 200 800 | 300 1000 | ps |
| V _{INPP} | Input Voltage Swing (Differential Configuration) (Note 14) | 100 | | 1200 | mV |
| Stabilization Time | Stabilization Time From Power-up VDD = 3.3 V to First Edge Out Upon Reprogram – (Pin-Strap mode), Change of Configuration Power-up to Static Output Levels – (Pin-Strap mode) Power-up to I ² C Ready | | 5 3 1 5 | 6 3 | ms |

t_{PWRDWN}

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Table 10. RECOMMENDED CRYSTAL SPECIFICATIONS

| Crystal | Fundamental AT-Cut |
|------------------------------|---------------------------|
| Frequency | 25 MHz |
| Load Capacitance | 16 pF – 20 pF |
| Shunt Capacitance, C0 | 7 pF Max |
| Equivalent Series Resistance | 50 Ω Max |

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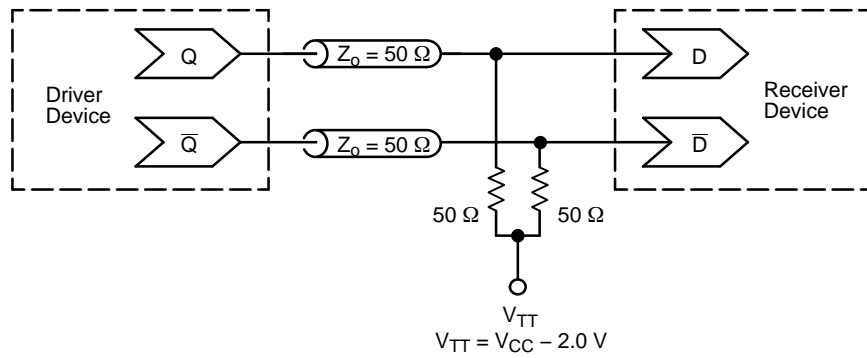
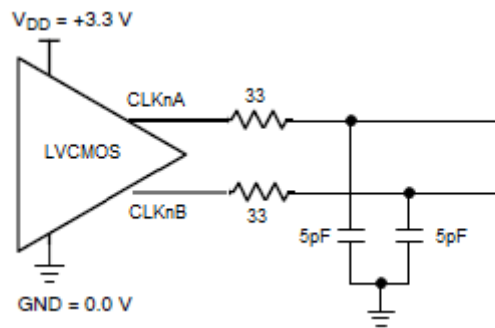
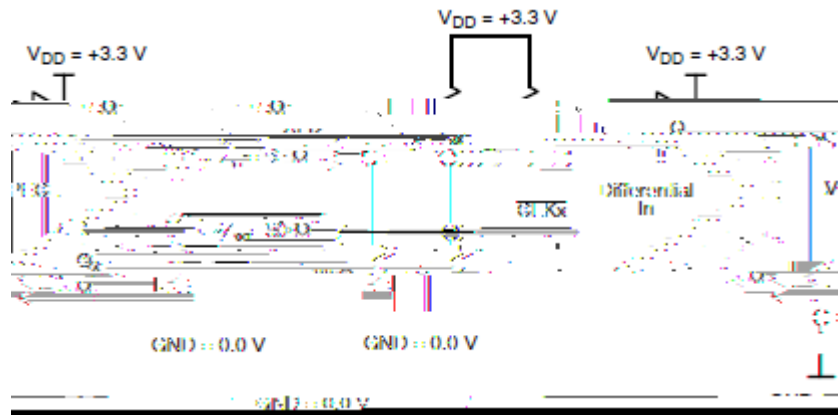


Figure 9. Typical Termination for LVPECL Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)



Interfacing from 3.3 V LVPECL to LVDS

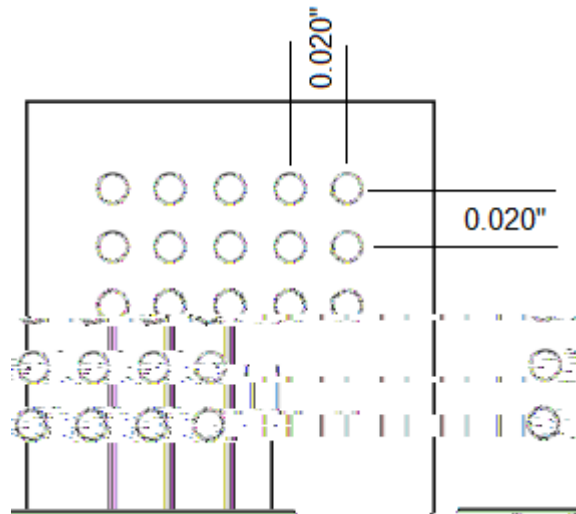
Since the output levels V_{OH} and V_{OL} of 3.3 V LVPECL are more positive than the input range of LVDS receiver, a special interface is required. (See Figures 12 and 13). Furthermore, the open emitter design of the ECL output structure needs proper termination, which can be implemented with a resistor divider network to generate proper LVDS DC levels (eq. 1).

$$R_{E1} + R_{E2} = R_E \quad (\text{eq. 1})$$

The resistor divider network will divide the output

Interfacing from 2.5 V LVPECL to LVDS

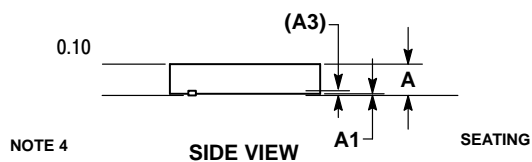
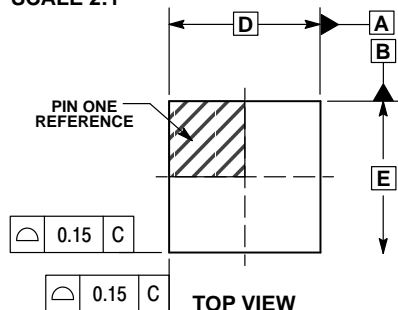
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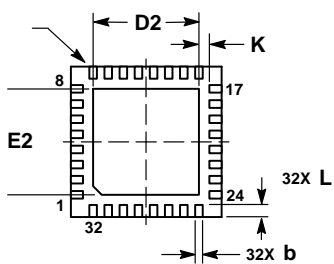
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CASE 485CE
ISSUE O

DATE 07 FEB 2012

SCALE 2:1

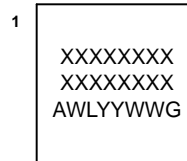


NOTE 4

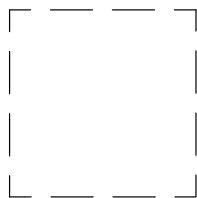


BOTTOM VIEW

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package



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