3.3 V 100/133 MHz Differential 1:12 HCSL orDA Differ

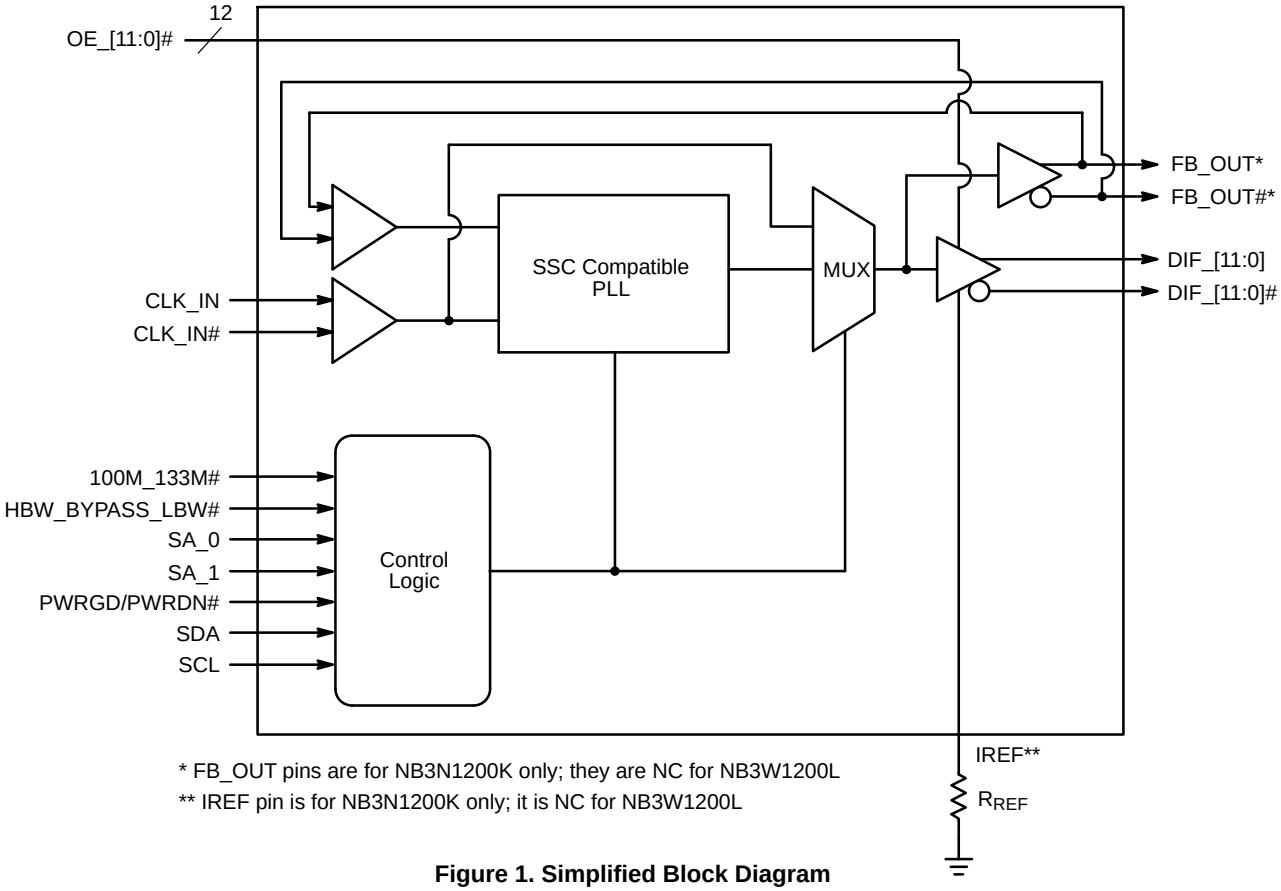
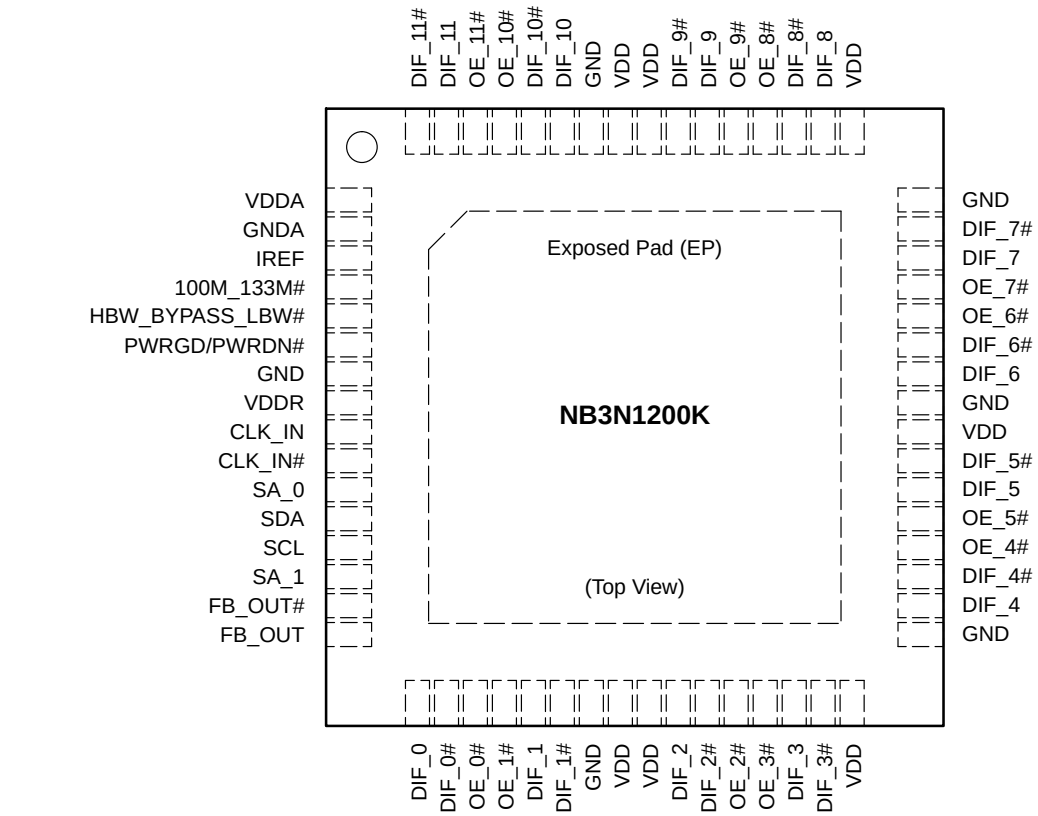


Figure 1. Simplified Block Diagram

PIN CONNECTIONS



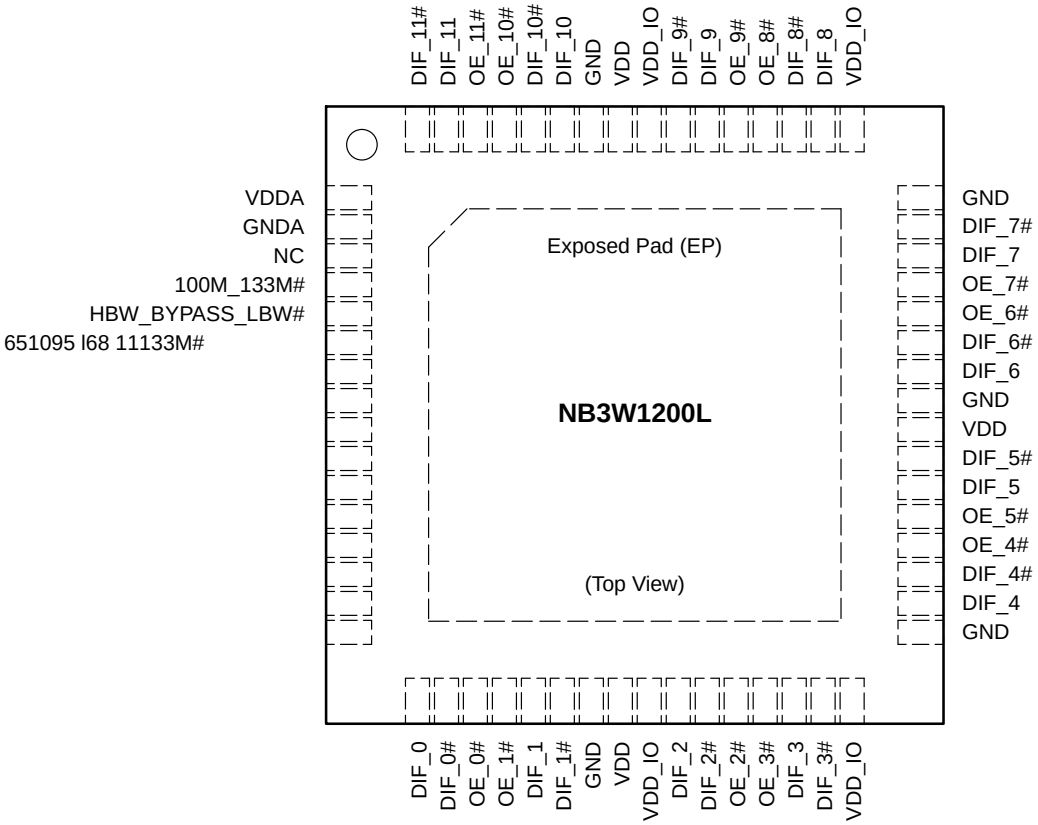


Table 1. NB3N1200K PIN DESCRIPTIONS

Pin Number	Pin Name	Type	Description
1	VDDA	3.3 V	3.3 V Power Supply for PLL.
2	GNDA	GND	Ground for PLL.
3	IREF	I	A precision resistor is attached to this pin to set the differential output current. Use R_{REF} = 475 Ω, 1% for 100 Ohms trace. Use R_{REF} = 412 Ω, 1% for 85 Ohms trace.
4	100M_133M#		

Table 1. NB3N1200K PIN DESCRIPTIONS

Pin Number	Pin Name	Type	Description
34	DIF_4	O, DIF	0.7 V Differential True clock output
35	DIF_4#	O, DIF	0.7 V Differential Complementary clock output
36	OE_4#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 4. 0 enables outputs, 1 disables outputs. Internal pull down.
37	OE_5#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 5. 0 enables outputs, 1 disables outputs. Internal pull down.
38	DIF_5	O, DIF	0.7 V Differential True clock output
39	DIF_5#	O, DIF	0.7 V Differential Complementary clock output
40	VDD	3.3 V	3.3 V power supply for outputs.
41	GND	GND	Ground for outputs.
42	DIF_6	O, DIF	0.7 V Differential True clock output
43	DIF_6#	O, DIF	0.7 V Differential Complementary clock output
44	OE_6#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 6. 0 enables outputs, 1 disables outputs. Internal pull down.
45	OE_7#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 7. 0 enables outputs, 1 disables outputs. Internal pull down.
46	DIF_7	O, DIF	0.7 V Differential True clock output
47	DIF_7#	O, DIF	0.7 V Differential Complementary clock output
48	GND	GND	Ground for outputs.
49	VDD	3.3 V	3.3 V power supply for outputs.
50	DIF_8	O, DIF	0.7 V Differential True clock output
51	DIF_8#	O, DIF	0.7 V Differential Complementary clock output
52	OE_8#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 8. 0 enables outputs, 1 disables outputs. Internal pull down.
53	OE_9#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 9. 0 enables outputs, 1 disables outputs. Internal pull down.
54	DIF_9	O, DIF	0.7 V Differential True clock output
55	DIF_9#	O, DIF	0.7 V Differential Complementary clock output
56	VDD	3.3 V	3.3 V power supply for outputs.
57	VDD	3.3 V	3.3 V power supply for outputs.
58	GND	GND	Ground for outputs.
59	DIF_10	O, DIF	0.7 V Differential True clock output
60	DIF_10#	O, DIF	0.7 V Differential Complementary clock output
61	OE_10#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 10. 0 enables outputs, 1 disables outputs. Internal pull down.
62	OE_11#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 11. 0 enables outputs, 1 disables outputs. Internal pull down.
63	DIF_11	O, DIF	0.7 V Differential True clock output
64	DIF_11#	O, DIF	0.7 V Differential Complementary clock output
EP	Exposed Pad	Thermal	The Exposed Pad (EP) on the QFN−64 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached th8v70022 Tc0<2 Tosed Pad

Table 2. NB3W1200L PIN DESCRIPTIONS

Pin Number	Pin Name	Type	Description
1	VDDA	3.3 V	3.3 V Power Supply for PLL.
2	GNDA	GND	Ground for PLL.
3	NC	I/O	No Connect
4	100M_133M#	I, SE	3.3 V tolerant inputs for input/output Frequency Selection (FS). An external pull−up or pull−down resistor is attached to this pin to select the input/output frequency. High = 100 MHz Output Low = 133 MHz Output
5	HBW_BYPASS_LBW#	I, SE	Tri−Level input for selecting the PLL bandwidth or bypass mode (refer to tri− level threshold in Table 4). High = High BW mode, Med = Bypass mode, Low = Low BW mode
6	PWRGD / PWRDN#	I	3.3 V LVTTL input to power up or power down the device.
7	GND	GND	Ground for outputs.
8	VDDR	VDD	3.3 V power supply for receiver.
9	CLK_IN	I, DIF	0.7 V Differential True input
10	CLK_IN#	I, DIF	0.7 V Differential Complementary input
11	SA_0	I	3.3 V LVTTL input selecting the address. Tri−level input (refer to tri−level threshold in Table 4.)
12	SDA	I/O	Open collector SMBus data.
13	SCL	I/O	SMBus slave clock input.
14	SA_1	I	3.3 V LVTTL input selecting the address. Tri−level input (refer to tri−level threshold in Table 4.)
15	NC	I/O	No Connect. There are active signals on pin 15; do not connect anything to this pin.
16	NC	I/O	No Connect. There are active signals on pin 16; do not connect anything to this pin.
17	DIF_0	O, DIF	0.7 V Differential True clock output
18	DIF_0#	O, DIF	0.7 V Differential Complementary clock output
19	OE_0#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 0. 0 enables outputs, 1 disables outputs. Internal pull down.
20	OE_1#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 1. 0 enables outputs, 1 disables outputs. Internal pull down.
21	DIF_1	O, DIF	0.7 V Differential True clock output
22	DIF_1#	O, DIF	0.7 V Differential Complementary clock output
23	GND	GND	Ground for outputs.
24	VDD	3.3 V	3.3 V power supply for core.
25	VDD_IO	VDD	Power supply for differential outputs.
26	DIF_2	O, DIF	0.7 V Differential True clock output
27	DIF_2#	O, DIF	0.7 V Differential Complementary clock output
28	OE_2#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 2. 0 enables outputs, 1 disables outputs. Internal pull down.
29	OE_3#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 3. 0 enables outputs, 1 disables outputs. Internal pull down.
30	DIF_3	O, DIF	0.7 V Differential True clock output
31	DIF_3#	O, DIF	0.7 V Differential Complementary clock output
32	VDD_IO	VDD	

Table 2. NB3W1200L PIN DESCRIPTIONS

Pin Number	Pin Name	Type	Description
34	DIF_4	O, DIF	0.7 V Differential True clock output
35	DIF_4#	O, DIF	0.7 V Differential Complementary clock output
36	OE_4#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 4. 0 enables outputs, 1 disables outputs. Internal pull down.
37	OE_5#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 5. 0 enables outputs, 1 disables outputs. Internal pull down.
38	DIF_5	O, DIF	0.7 V Differential True clock output
39	DIF_5#	O, DIF	0.7 V Differential Complementary clock output
40	VDD	3.3 V	3.3 V power supply for core.
41	GND	GND	Ground for outputs.
42	DIF_6	O, DIF	0.7 V Differential True clock output
43	DIF_6#	O, DIF	0.7 V Differential Complementary clock output
44	OE_6#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 6. 0 enables outputs, 1 disables outputs. Internal pull down.
45	OE_7#	I, SE	3.3 V LVTTL active low input for enabling DIF output pair 7. 0 enables outputs, 1 disables outputs. Internal pull down.
46	DIF_7	O, DIF	0.7 V Differential True clock output
47			

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition	Min	Max	Units
$V_{DD}/V_{DDA}/V_{DDR}$	Core Supply Voltage			4.6	V
V_{DD_IO}	I/O Supply Voltage			4.6	V
[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	V
[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	V
[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	V
[redacted]	[redacted]	[redacted]	[redacted]	[redacted]	°C

NB3N1200K / NB3W1200L OUTPUT RELATIONAL TIMING PARAMETERS

Table 5. ELECTRICAL CHARACTERISTICS Skew and Differential Jitter Parameters

(V_{DD} = V_{DDA} = V_{DDR} = 3.3 V ±5%, T_A = 0 − 70°C)

Group	Description	Min	Typ	Max	Units
CLK_IN, DIF[x:0] (Notes 9, 10, 12, 13)	Input−to−Output Delay in PLL mode, nominal value	−100		100	ps
CLK_IN, DIF[x:0] (Notes 10, 11, 13)	Input−to−Output Delay in Bypass mode, nominal value	2.5		4.5	ns
CLK_IN, DIF[x:0] (Notes 10, 11, 13)	Input−to−Output Delay variation in PLL mode (over voltage and temperature), nominal value			|100|	ps
CLK_IN, DIF[x:0] (Notes 10, 11, 13)	Input−to−Output Delay variation in Bypass mode (over voltage and temperature), nominal value			|250|	ps
DIF[11:0] (Notes 9, 10, 11, 13)	Output−to−Output Skew across all 12 outputs (Common to Bypass and PLL mode)	0		50	ps

9. Measured into fixed 2 pF load capacitance. Input to output skew is measured at the first output edge following the corresponding input.
10. Measured from differential cross−point to differential cross−point.
11. All Bypass Mode Input−to−Output specs refer to the timing between an input edge and the specific output edge created by it.
12. This parameter is deterministic for a given device.
13. Measured with scope averaging on to find mean value.

Table 10. CLOCK PERIOD SSC DISABLED

SSC OFF Center Freq. MHz	Measurement Window							Units
	1 Clock	1 μs	0.1 s	0.1 s	0.1 s	1 μs	1 Clock	
	Jitter c c Abs Per Min	SSC Short Avg Min	ppm Long Avg Min	0 ppm Period	+ ppm Long Avg Max	+ SSC Short Avg Max	+ Jitter c c Abs Per Max	
100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns
133.33	7.44925		7.49925	7.50000	7.50075		7.55075	ns

Table 11. CLOCK PERIOD SSC ENABLED

SSC ON Center Freq. MHz	Measurement Window							Units
	1 Clock	1 μs	0.1 s	0.1 s	0.1 s	1 μs	1 Clock	
	Jitter c c Abs Per Min	SSC Short Avg Min	ppm Long Avg Min	0 ppm Period	+ ppm Long Avg Max	+ SSC Short Avg Max	+ Jitter c c Abs Per Max	
99.75	9.94900	9.99900	10.02406	10.02506	10.02607	10.05126	10.10126	ns
133.00	7.44925	7.49925	7.51805	7.51880	7.51955	7.53845	7.58845	ns

Table 12. INPUT EDGE RATE (Note 46)

Frequency Select (FS)	Min	Max	Unit
100 MHz	0.35	N/A	V/ns
133 MHz	0.35	N/A	V/ns

46. Input edge rate is based on single ended measurement. This is the minimum input edge rate at which the NB3N1200K / NB3W1200L devices are guaranteed to meet all performance specifications.

MEASUREMENT POINTS FOR DIFFERENTIAL

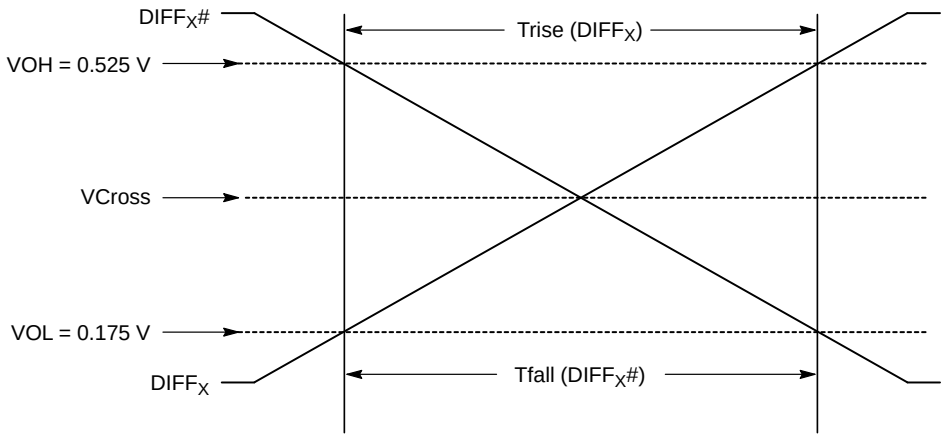


Figure 4. Single Ended Measurement Points for Trise, Tfall

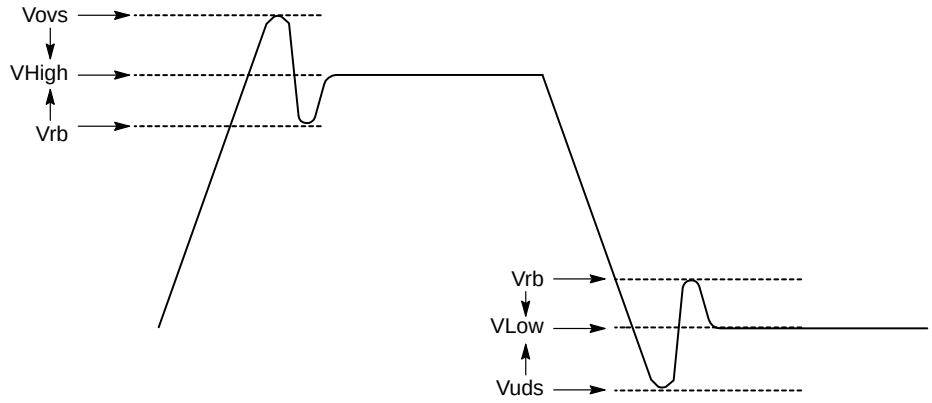


Figure 5. Single Ended Measurement Points for Vovs, Vuds, Vrb

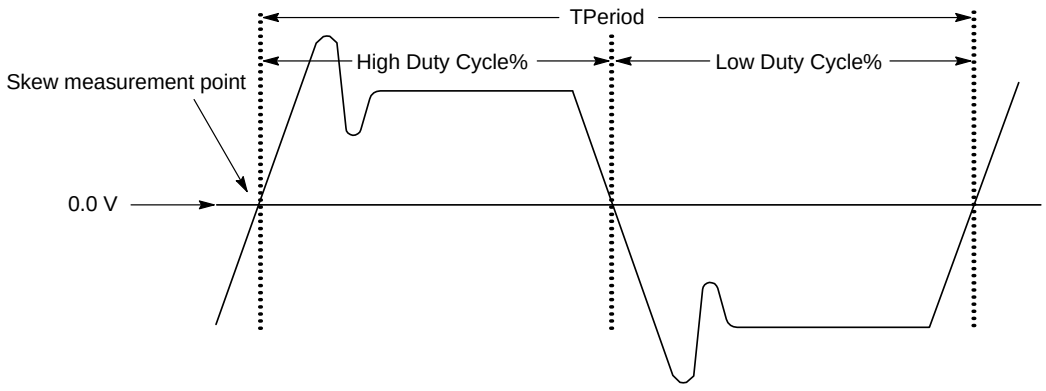
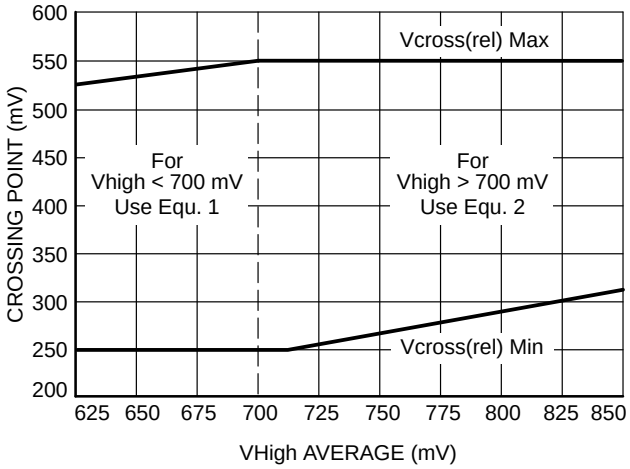


Figure 6. Differential (DIFF$_X$ – DIFF$_X$#) Measurement Points (Tperiod, Duty Cycle, Jitter)



Equ 1: Vcross(rel) Max = 0.550 − 0.5(0.7 − Vhavg)
Equ 2: Vcross(rel) Min = 0.250 + 0.5(Vhavg − 0.7)

Figure 7. Vcross Range Clarification

The picture above illustrates the effect of Vhigh above and below 700 mV on the Vcross range. The purpose of this is to prevent a 250 mV Vcross with an 850 mV Vhigh. In addition, this prevents the case of a 550 mV Vcross with a 660 mV Vhigh. The actual specification for Vcross is dependent upon the measured amplitude of Vhigh.

CLK_IN, CLK_IN#

The differential input clock is expected to be sourced from a clock synthesizer.

OE# and Output Enables (Control Registers)

Each output can be individually enabled or disabled by SMBus control register bits. Additionally, each output of the DIF[11:0] has a dedicated OE# pin. The OE# pins are asynchronous asserted−low signals. The Output Enable bits in the SMBus registers are active high and are set to enable by default.

The disabled state for the NB3N1200K HCSL outputs is Hi−Z, with the termination network pulling the outputs Low/Low. The disabled state for the NB3W1200L low power NMOS Push−Pull outputs is Low/Low. In the following text, if the NB3N1200K HCSL output is referred to as Hi−Z or Tri− state, the equivalent state of the NB3W1200L NMOS Push−pull output is Low/Low.

Please note that the logic level for assertion or deassertion is different in software than it is on hardware. This follows hardware default nomenclature for communication channels (e.g., output is enabled if OE# pin is pulled low) and still maintains software programming logic (e.g., output is enabled if OE register is true).

Please refer to Table 13 for the truth table for enabling and disabling outputs via hardware and software. Note that both the control register bit must be a ‘1’ AND the OE# pin must be a ‘0’ for the output to be active.

NOTE: The assertion and de−assertion of this signal is absolutely asynchronous.

Table 13. NB3N1200K OE AND POWER MANAGEMENT

Inputs		OE# Hardware Pins & Control Register Bits			Outputs	
PWRGD/ PWRDN#	CLK_IN/ CLK_IN#	SMBUS Enable Bit	OE# Pin	DIF/DIF# [11:0]	FB_OUT/ FB_OUT#	PLL State
0	X	X	X	Hi−Z	Hi−Z	OFF
1	Running	0	X	Hi−Z	Running	ON
		1	0	Running	Running	ON
		1	1	Hi−Z	Running	ON

Table 14. NB3W1200L POWER MANAGEMENT

Inputs		OE# Hardware Pins & Control Register Bits			Outputs	
PWRGD/ PWRDN#	CLK_IN/ CLK_IN#	SMBUS Enable Bit	OE# Pin	DIF/DIF# [11:0]	NC pins (Pins 15, 16)	PLL State
0	X	X	X	Low/Low	Low/Low	OFF
1	Running	0	X	Low/Low	Running	ON
		1	0	Running	Running	ON
		1				

OE# Assertion (Transition from ‘1’ to ‘0’)

All differential outputs that were tri−stated are to resume normal operation in a glitch free manner. The latency from the assertion to active outputs is 4 − 12 DIF clock periods.

OE# De-Assertion (Transition from ‘0’ to ‘1’)

The impact of de−asserting OE# is each corresponding output will transition from normal operation to tri−state in a glitch free manner. A minimum of 4 valid clocks will be provided after the de−assertion of OE#. The maximum latency from the de−assertion to tri−stated outputs is 12 DIF clock periods.

100M_133M# Frequency Selection (FS)

The NB3N1200K / NB3W1200L is optimized for lowest phase jitter performance at 100 MHz and 133 MHz operating frequencies. The 100M_133M# is a hardware pin, which programs the appropriate output frequency of the DIF pairs. Note that the CLK_IN frequency is equal to CLK_OUT frequency; this means that the NB3N1200K / NB3W1200L is operated in the 1:1 mode only. The Frequency Selection can be enabled by the 100M_133M# hardware pin.

Buffer Power Up State Machine

Table 18. BUFFER POWER UP STATE MACHINE

State	Description
0	3.3 V Buffer power off
1	After 3.3 V supply is detected to rise above 3.135 V, the buffer enters State 1 and initiates a 0.1 ms–0.3 ms delay.
2	Buffer waits for a valid clock on the CLK input and PWRDN# de−assertion (or PWRGD assertion low to high)
3	Once the PLL is locked to the CLK_IN input clock, the buffer enters state 3 and enables outputs for normal operation. (Notes 47, 48)

47. The total power up latency from power on to all outputs active must be less than 1.8 ms (assuming a valid clock is present on CLK_IN input).
48. If power is valid and powerdown is de−asserted (PWRGD asserted) but no input clocks are present on the CLK_IN input, DIF clocks must remain disabled. Only after valid input clocks are detected, valid power, PWRDN# de−asserted (PWRGD asserted) with the PLL locked/stable and the DIF outputs enabled.

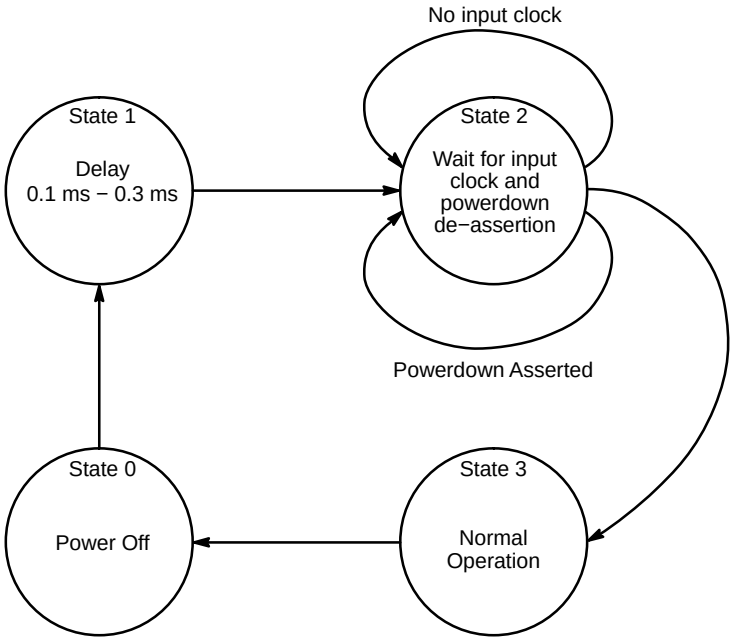


Figure 8. Buffer Power Up State Diagram

Device Power Up Sequence

Follow the power−up sequence below for proper device functionality:

1. PWRGD/PWRDN# pin must be Low.
2. Assign remaining control pins to their required

PWRDN# Assertion

When PWRDN# is sampled low by two consecutive rising edges of DIF#, all differential outputs must held tri-stated on the

Byte Read/Write

Reading or writing a register in a SMBus slave device in byte mode always involves specifying the register number.

Read. The standard byte read is as shown in the following figure. It is an extension of the byte write. The write start condition is repeated then the slave device starts sending data and the master acknowledges it until the last byte is sent. The master terminates the transfer with a NAK, then a stop condition. For byte operation, the $2*7^{th}$ bit of the command byte must be set. For block operations, the $2*7^{th}$ bit must be reset. If the bit is not set, the next byte must be the byte transfer count.

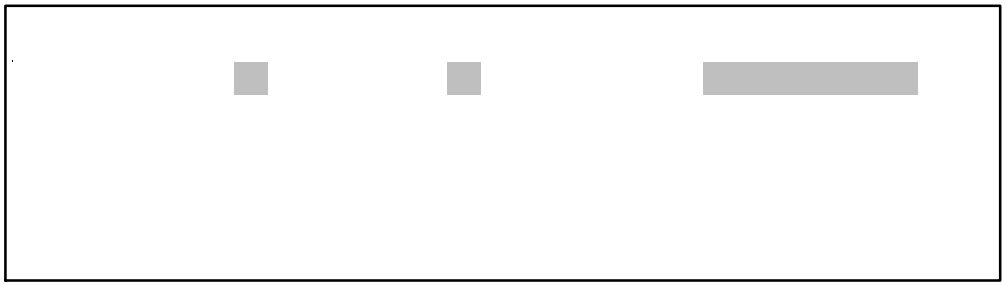


Figure 13. Byte Read Protocol

Write. After the slave address is sent with the r/w condition bit not set, the command byte is sent with the MSB = 0. The lower seven bits indicate what register to start the transfer at. If the command byte is 00h, the slave device will be compatible with existing block mode slave devices. The next byte of a write must be the count of bytes that the master will transfer to the slave device. The byte count must be greater than zero and less than 33. Following this byte are the data bytes to be transferred to the slave device. The slave device always acknowledges each byte received. The transfer is terminated after the slave sends the Ack and the master sends a stop function.

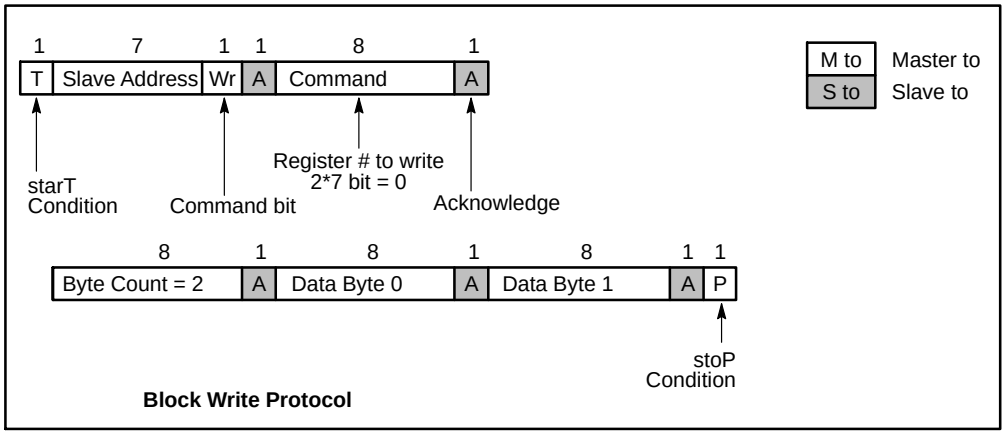


Figure 16. Block Write Protocol

NB3N1200K/NB3W1200L CONTROL REGISTER

Table 21. BYTE **0**: FREQUENCY SELECT, OUTPUT ENABLE, PLL MODE CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	100M_133M# Frequency Select (FS)	133 MHz	100 MHz	R	Latched at power up	DIF[11:0]
1	PLL Mode 0	See PLL Operating Mode Readback Table		RW		

Table 22. BYTE 1: OUTPUT ENABLE CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable DIF 0	Hi−Z for NB3N1200K Low/Low for NB3W1200L	Enabled	RW	1	DIF_0, DIF_0#
1	Output Enable DIF 1	Hi−Z for NB3N1200K Low/Low for NB3W1200L	Enabled	RW	1	DIF_1, DIF_1#
2	Output Enable DIF 2	Hi−Z for NB3N1200K Low/Low for NB3W1200L	Enabled	RW	1	DIF_2, DIF_2#
3	Output Enable DIF 3	Hi−Z for NB3N1200K Low/Low for NB3W1200L	Enabled	RW	1	DIF_3, DIF_3#
4	Output Enable DIF 4	Hi−Z for NB3N1200K Low/Low for NB3W1200L	Enabled	RW	1	DIF_4, DIF_4#
5	Output Enable DIF 5	Hi−Z for NB3N1200K Low/Low for NB3W1200L	Enabled	RW	1	DIF_5, DIF_5#
6	Output Enable DIF 6	Hi−Z for NB3N1200K Low/Low for NB3W1200L	Enabled	RW	1	DIF_6, DIF_6#
7	Output Enable DIF 7	Hi−Z for NB3N1200K Low/Low for NB3W1200L	Enabled	RW	1	DIF_7, DIF_7#

Table 23. BYTE 2: OUTPUT ENABLE CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable DIF 8	Hi−Z for NB3N1200K Low/Low for NB3W1200L	Enabled	RW	1	DIF_8, DIF_8#
1	Output Enable DIF 9	Hi−Z for NB3N1200K Low/Low for NB3W1200L	Enabled	RW	1	DIF_9, DIF_9#
2	Output Enable DIF 10	Hi−Z for NB3N1200K Low/Low for NB3W1200L	Enabled	RW	1	DIF_10, DIF_10#
3	Output Enable DIF 11	Hi−Z for NB3N1200K Low/Low for NB3W1200L	Enabled	RW	1	DIF_11, DIF_11#

Table 27. BYTE 6: DEVICE ID CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	1200K	1200L
0	Device ID 0	1200K = 120d = 78hex 1200L = 130d = 82hex		R	0	0
1	Device ID 1			R	0	1
2	Device ID 2			R	0	0
3	Device ID 3			R	1	0
4	Device ID 4			R	1	0
5	Device ID 5			R	1	0
6	Device ID 6			R	1	0

Table 30. DIF CLOCK OUTPUT CURRENT

Board Target Trace/Term Z	Reference R, $I_{ref} = V_{DD}/(3*R_r)$	Output Current	V_{OH} @ Z

Termination of Differential Outputs

Table 31. NB3N1200K RESISTIVE LUMPED TEST LOADS FOR DIFFERENTIAL CLOCKS

Clock	Board Trace Impedance	R_s	R_p	RI_{ref}	Units
DIFF Clocks – 50 Ω configuration	100	33 5%	49.9 1%	475 1%	Ω
DIFF Clocks – 43 Ω configuration	85	27 5%	42.2 1%	412 1%	Ω

Table 32. NB3W1200L RESISTIVE LUMPED TEST LOADS FOR DIFFERENTIAL CLOCKS

Clock	Board Trace Impedance	R_s	R_p	RI_{ref}	Units
DIFF Clocks – 50 Ω configuration	100	33 5%	N/A	N/A	Ω
DIFF Clocks – 43 Ω configuration	85	27 5%	N/A	N/A	Ω

Termination of Differential HCSL Type **Outputs (NB3N1200K)**

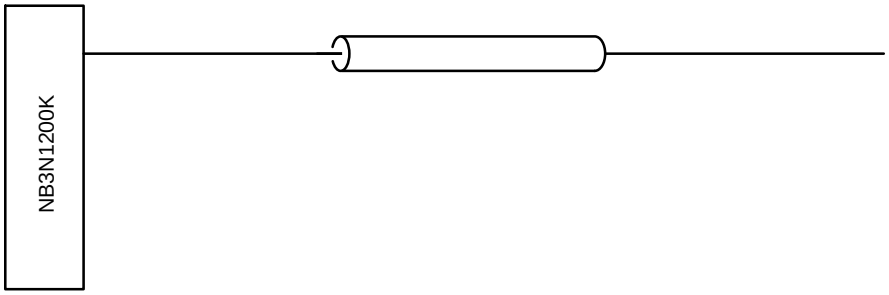
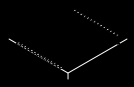


Figure 19. 0.7 V Configuration Test Load Board Termination for HCSL NB3N1200K



XXXXXXXXX
XXXXXXXXX
AWLYYWWG

XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “▪”, may or may not be present.