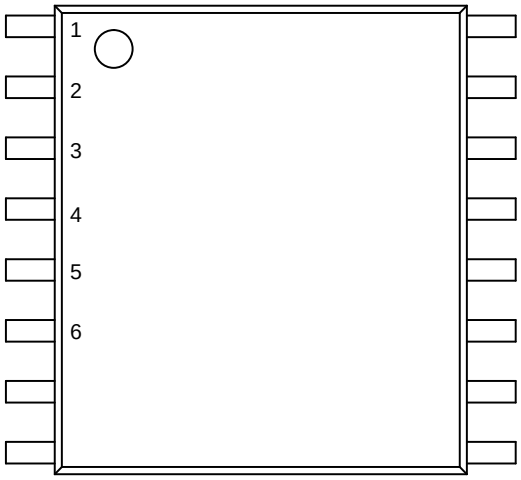

1
2
3
4
5
6

Table 3. ATTRIBUTES

Characteristic		Value
ESD Protection	Human Body Model	> 2 kV
RPU − OE, SEL0 and SEL1 Pull−up Resistor		100 kΩ
Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		7623
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{DD}	Positive Power Supply	GND = 0 V		4.6	V
V_I	Input Voltage (V_{IN})	GND = 0 V	$GND \le V_I \le V_{DD}$	−0.5 V to V_{DD}+0.5 V	V
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}					

Table 7. AC ELECTRICAL CHARACTERISTICS − PCI EXPRESS JITTER SPECIFICATIONS,
V_{DD} = 3.3 V ± 5%, T_A = −40°C to 85°C

Symbol	Parameter	Conditions (Notes 10 and 11)	Min	Typ	Max	Industry Limit	Unit
$t_{jphPCIeG1}$	RMS Phase Jitter	PCIe Gen 1 (Notes 12 and 13)		10	16	86	ps (p−p)
$t_{jphPCIeG2}$		PCIe Gen 2 Lo Band 10 kHz < f < 1.5 MHz (Note 12)		0.2	0.25	3	ps (rms)
		PCIe Gen 2 High Band 1.5 MHz < f < Nyquist (50 MHz) (Note 12)		0.9	1.2	3.1	ps (rms)
$t_{jphPCIeG3}$		PCIe Gen 3 (PLL BW of 2−4 MHz, CDR = 10 MHz) (Note 12)		0.2	0.3	1	ps (rms)
$t_{jphPCIeG4}$		PCIe Gen 4 (PLL BW of 2−4 MHz, CDR = 10 MHz) (Note 12)		0.21	0.3	0.5	ps (rms)
t_{jphUPI}		UPI (9.6 Gb/s, 10.4 Gb/s or 11.2 Gb/s, 100 MHz, 12 UI)		0.62	0.7	1.0	ps (rms)
t_{jphQPI_SMI}		QPI & SMI (100.00 MHz or 133.33 MHz, 4.8 Gb/s, 6.4 Gb/s 12UI) (Note 14)		0.1	0.3	0.5	ps (rms)
		QPI & SMI (100.00 MHz, 8.0 Gb/s, 12UI) (Note 14)		0.1	0.15	0.3	ps (rms)
		QPI & SMI (100.00 MHz, 9.6 Gb/s, 12UI) (Note 14)		0.07	0.1	0.2	ps (rms)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
10. Applies to all outputs.
11. Guaranteed by design and characterization, not tested in production
12. See http://www.pcisig.com for complete specs
13. Sample size of at least 100K cycles. This figures extrapolates to 108 ps pk−pk @ 1M cycles for a BER of 1−12.
14. Calculated from Intel−supplied Clock Jitter Tool v 1.6.3.

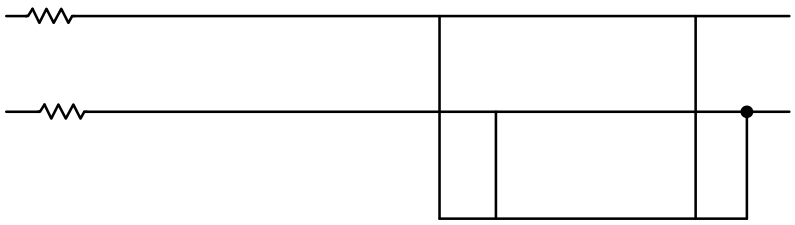
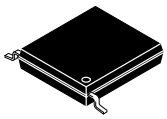


Figure 3. Typical Termination for Output Driver and Device Evaluation



SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006