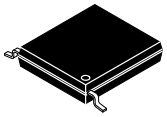
3.3 V, LVPECL/LVCMOS Clock Multiplier

NB3N3020



TSSOP−16
DT SUFFIX
CASE 948F

MARKING DIAGRAM

Description

The NB3N3020 is a high precision, low phase noise selectable clock multiplier. The device takes a 5 – 27 MHz fundamental mode parallel resonant crystal or a 2 − 210 MHz LVCMOS single ended clock source and generates a differential LVPECL output and a single ended LVCMOS/LVTTL output at a selectable clock output frequency which is a multiple of the input clock frequency. Three tri−level (Low, Mid, High) LVCMOS/LVTTL single ended select pins set one of 26 possible clock multipliers. The LVCMOS/LVTTL output enable (OE1) tri−states the LVCMOS/LVTTL clock output (CLK1) when low. When the LVTTL/LVCMOS output enable (OE2) is LOW, LVPECL CLK2 is forced LOW and LVPECL $\overline{CLK2}$ is forced HIGH.

This device is housed in 5 mm x 4.4 mm narrow body TSSOP 16 pin package.

Features

- Selectable Clock Multiplier
- External Loop Filter is Not Required
- LVPECL Differential Output
- LVCMOS/ LVTTL Outputs
- RMS Period Jitter of 5 ps
- Jitter or Low Phase Noise at 125 MHz [25 MHz Input]:

100 Hz	−95 dBc/Hz
1 kHz	−107 dBc/Hz
10 kHz	−112 dBc/Hz
100 kHz	−117 dBc/Hz
1 MHz	−117 dBc/Hz
10 MHz	−134 dBc/Hz

- Operating Range 3.3 V ±10%
- Industrial Temperature Range −40°C to +85°C
- These are Pb−Free Devices

ORDERING INFORMATION

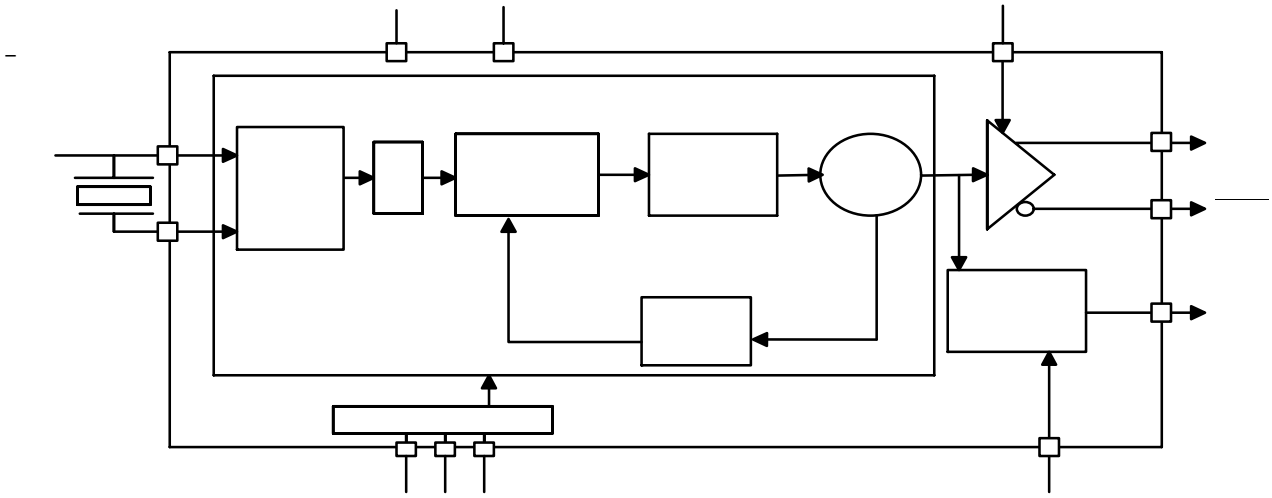


Figure 1. NB3N3020 Simplified Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description

become active synchronous to the internal PLL output clock and do not create any glitches or runt pulses during the transition. In power down mode, the outputs are tri−stated regardless of the state of the OE1, OE2.

The device has an output enable [OE1] which accepts LVTTL/LVCMOS levels and when set LOW will disable the LVTTL/LVCMOS level CLK1 to tri − state. Output enable OE2 accepts LVTTL/LVCMOS levels to disable the LVPECL level outputs by forcing CLK2 LOW and CLK2b HIGH. When OE1 or OE2 are set LOW (Disabled), the PLL remains running while the respective clock outputs are disabled. When the OE1 or OE2 are set enabled (HIGH), the clock outputs become active synchronous to the internal PLL output clock and will not create any glitches or runt pulses during the transition. Both OE1 and OE2 inputs have pull−up resistors which default to VDD when floated open. In power down mode, the outputs are tri − stated (zero current) regardless of the state of the OE1, OE2.

Changing Clock Multiplier

The clock output frequency can be dynamically changed using Sel0, Sel1, Sel2 pins. When the clock frequency is changed, the clock outputs move from one frequency to another and the PLL locks to the new frequency within a settling time of 3 msec. There is no glitch during this transition when the clock outputs are active {not tri−stated by OE1, OE2}.

Crystal/ Clock Input

The device takes in a 5 – 27 MHz crystal input or 2 – 210 MHz clock input. Once powered up, the input frequency is fixed and should not be changed dynamically. The input cannot accept a spread spectrum clock and needs a fixed frequency clock for device operation. The input frequencies for clock and crystal input for specific multipliers are determined by Table 3.

Power Up

When the NB3N3020 is powered up, it takes 10 msec for the PLL's to stabilize and lock to the desired frequency of operation as selected by Sel0, Sel1, Sel2. During this time period, there may be glitches in the clock outputs.

Power Down:

The device can be powered down when the Sel0, Sel1, Sel2 pins are all connected to GND. In this mode of operation, PLL is turned off and the device consumes less than 5 mA of current. There may be a glitch in clock outputs when the device is powering down. In power down mode, the outputs are tri−stated regardless of the state of the OE1, OE2.

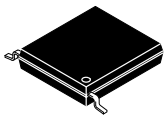
In the cases where the application requires glitch−less transitions, in order to avoid glitches it is recommended to use synchronous OE signaling to mask glitches to the clock outputs.

Table 3. ATTRIBUTES

Characteristics	Value

Table 6. AC CHARACTERISTICS ± – ° °

Symbol	Characteristic	Min



SCALE 2:1

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