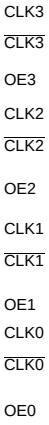
CLK3
CLK3
OE3
CLK2
CLK2
OE2
CLK1
CLK1
OE1
CLK0
CLK0
OE0

PIN DESCRIPTION

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	REF_SEL	Input	LVCMOS/ LVTTL level input to select input reference source. Pulldown with crystal as default reference input source.
2	REF_IN	Input	25 MHz single ended reference input clock.
3	V_{DD}	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.
4	GND	Ground	Power supply ground 0 V. This pin provides GND return path for the device.
5	XIN	Input	25 MHz fundamental mode crystal input connection. Ground this pin when crystal not connected.
6	XOUT	Output	25 MHz crystal output. Float this pin when crystal not connected.
7	MR_OE#	Input	Asynchronous LVCMOS/ LVTTL level input. When High, this pin acts as Master Reset to disable the output dividers and set outputs to high impedance (Hi Z) mode. When Low, this pin acts as Output Enable for enabling the output buffers. Pulldown with default Low.
8	V_{DD}	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.
9	OE3	Input	LVCMOS/ LVTTL level interface active High output enable pin for CLK3. Pulldown with default Low and output disabled.
10	OE2	Input	LVCMOS/ LVTTL level interface active High output enable pin for CLK2. Pulldown with default Low and output disabled.
11	OE1	Input	LVCMOS/ LVTTL level interface active High output enable pin for CLK1. Pulldown with default Low and output disabled.
12	OE0	Input	LVCMOS/ LVTTL level interface active High output enable pin for CLK0. Pulldown with default Low and output disabled.
13	GND	Ground	Power supply ground 0 V. This pin provides GND return path for the device.
14	V_{DD}	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.
15	CLK0	HCSL or LVDS output	Noninverted clock output. (For LVDS levels see Figure 10)
16	$\overline{CLK0}$	HCSL or LVDS output	Inverted clock output. (For LVDS levels see Figure 10)
17	CLK1	HCSL or LVDS output	Noninverted clock output. (For LVDS levels see Figure 10)
18	$\overline{CLK1}$	HCSL or LVDS output	Inverted clock output. (For LVDS levels see Figure 10)
19	GND	Ground	Power supply ground 0 V. This pin provides GND return path for the device.
20	CLK2	HCSL or LVDS output	Noninverted clock output. (For LVDS levels see Figure 10)
21	$\overline{CLK2}$	HCSL or LVDS output	Inverted clock output. (For LVDS levels see Figure 10)
22	CLK3	HCSL or LVDS output	Noninverted clock output. (For LVDS levels see Figure 10)
23	$\overline{CLK3}$	HCSL or LVDS output	Inverted clock output. (For LVDS levels see Figure 10)
24	V_{DD}	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.
25	F_SEL	Input	LVCMOS/ LVTTL level Frequency Selects PCIe (100 MHz) when Low or sRIO (125 MHz) output frequency when High. Pulldown with default of 100 MHz at outputs.
26	IREF	Output	Output current reference pin. Connect to precision resistor (typical 475 Ω) to set internal current reference
27	BYPASS	Input	LVCMOS/ LVTTL level input. Selects PLL operation mode when Low or PLL bypass mode when High. Pulldown with default of PLL mode.
28	V_{DD}	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.

Table 2. OUTPUT FREQUENCY SELECT FUNCTION TABLE

Input		Output
F_SEL	N (Output divider)	CLK[3:0]/CLK[3:0]#
0	5	100MHz (PCIe, default)
1	4	125MHz (sRIO)

Table 3. PLL BYPASS FUNCTION TABLE

BYPASS	PLL Configuration
0	PLL Enabled (default)
1	PLL bypassed, $f_{out} = f_{IN}/N$

Table 4. MASTER RESET AND OE FUNCTION TABLE

MR_OE#	OEx [x=3:0]	Function
0 (default)	0 (default)	CLKx, CLKx# are High impedance
	1	CLKx Output Enabled
1	x	Device reset, outputs disabled (Hi Z)

Table 5. INPUT REFERENCE SELECT FUNCTION TABLE

REF_SEL	Input Reference
0	Crystal, at XIN and XOUT (default)
1	Single ended reference clock at REF_IN

Recommended Crystal Parameters

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Ω

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Table 6. ATTRIBUTES

Characteristic		Value
ESD Protection	Human Body Model	2 kV
Internal Input Default State Resistor		51 kΩ
Moisture Sensitivity, Indefinite Time Out of Dray Pack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V 0 @ 0.125 in
Transistor Count		132,000
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 7. ABSOLUTE MAXIMUM RATING (Note 2)

Symbol	Parameter	Rating	Unit
V_{DD}	Positive power supply with respect to GND	+4.6	V

Table 8. DC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3 V ± 5%, GND = 0 V, T_A = 40°C to 85°C, Note 4)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage	3.135	3.3	3.465	V
I_{DD}	Power Supply Current when all outputs are ON, OE[3:0] = 1, F_{CLKOUT} = 125 MHz			126	mA
I_{OFF}	Power Supply Current when all outputs are set OFF, OE[3:0] = 0		45	50	mA
V_{IH}	Input HIGH Voltage (XIN, REF_IN, REF_SEL, BYPASS, F_SEL, MR_OE#)	2.0		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage (XIN, REF_IN, REF_SEL, BYPASS, F_SEL, MR_OE#)	GND 0.3		0.8	V
I_{IH}	Input Leackage on logic High current at all input pins			150	

Table 9. AC ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3 V ± 5%, GND = 0 V, T_A = 40°C to 85°C, Note 12)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLKIN}	Clock/ Crystal input frequency			25		

NB3N51044

PHASE NOISE

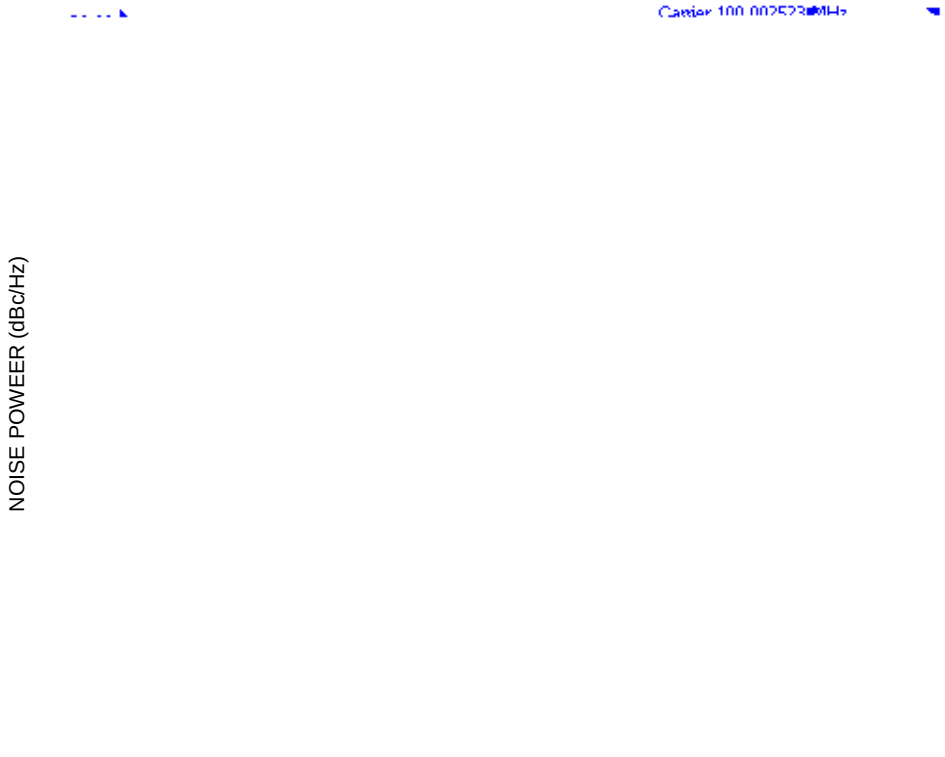

Figure 3. Typical Phase Noise Plot at 100 MHz (f_{CLKIN} = 25 MHz Crystal , f_{CLKOUT} = 100 MHz, RMS Phase Jitter = 172 fs for Integration Range of 1.875 MHz to 20 MHz, Output Termination = HCSL type)

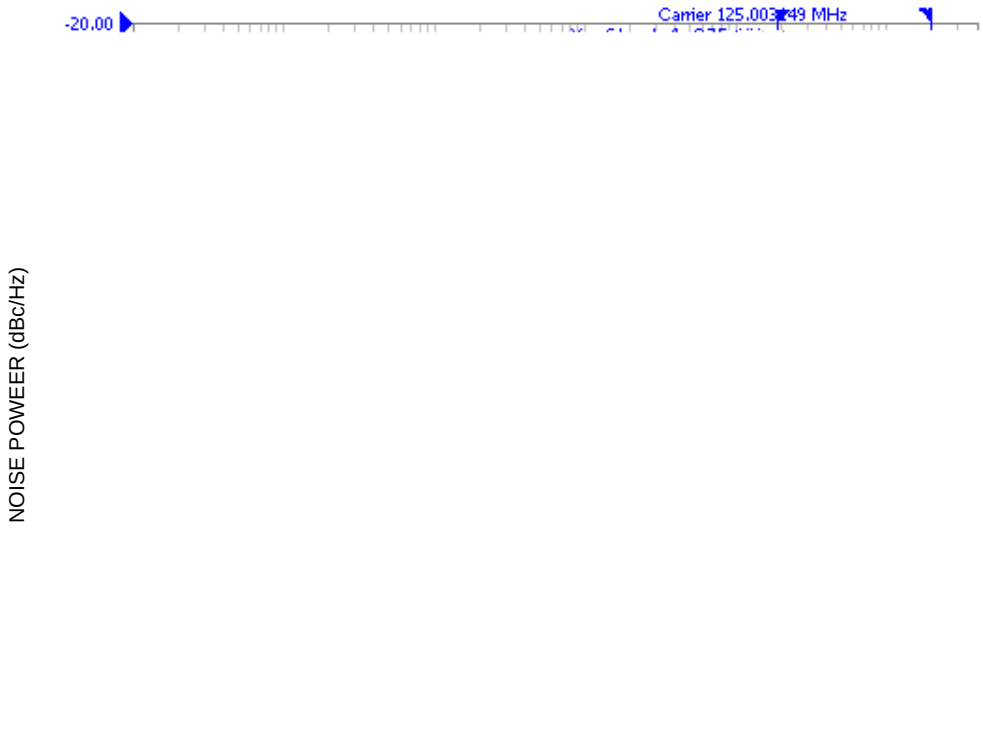

Figure 4. Typical Phase Noise Plot at 125 MHz (f_{CLKIN} = 25 MHz Crystal , f_{CLKOUT} = 125 MHz, RMS Phase Jitter = 155 fs for Integration Range of 1.875 MHz to 20 MHz, Output Termination = HCSL type)

PHASE NOISE

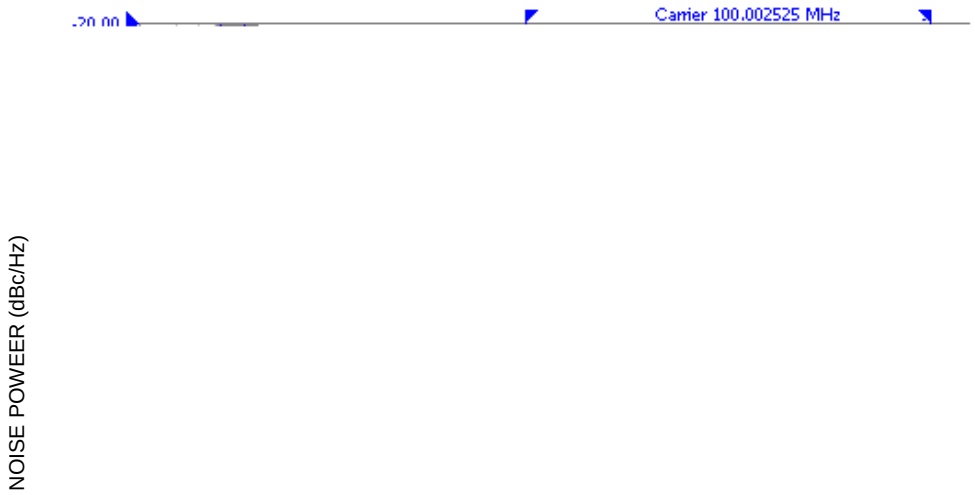

Figure 5. Typical Phase Noise Plot at 100 MHz (f_{CLKIN} = 25 MHz Crystal , f_{CLKOUT} = 100 MHz, RMS Phase Jitter = 389 fs for Integration Range of 12 kHz to 20 MHz, Output Termination = HCSL type)

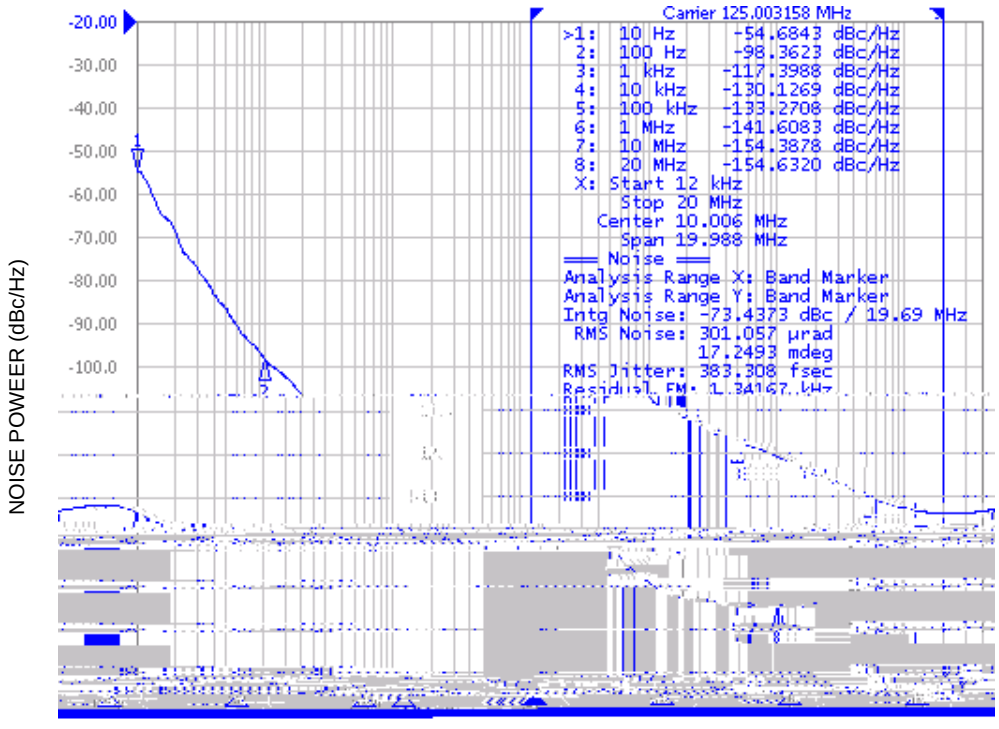

Figure 6. Typical Phase Noise Plot at 125 MHz (f_{CLKIN} = 25 MHz Crystal , f_{CLKOUT} = 125 MHz, RMS Phase Jitter = 383 fs for Integration Range of 12 kHz to 20 MHz, Output Termination = HCSL type)

APPLICATION INFORMATION

Crystal Input Interface

Figure 7. Crystal Interface Loading

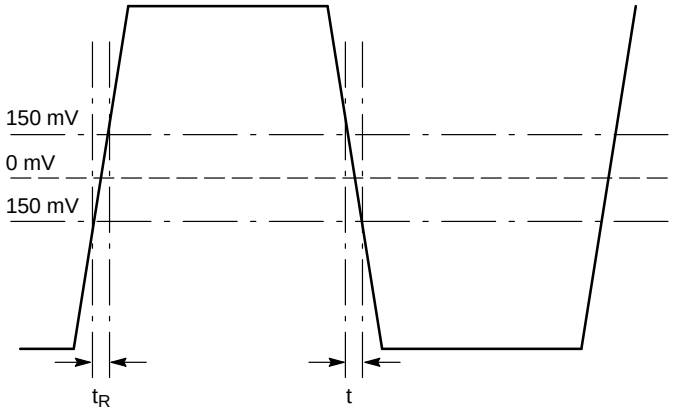

Figure 11. HCSL Differential Measurement of t_R/t_F

TSSOP28
CASE 948AA
ISSUE A

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