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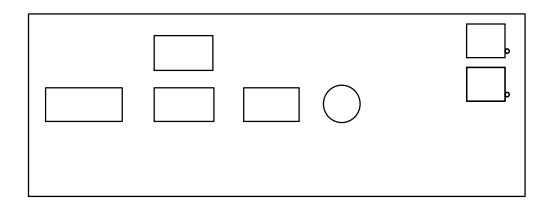


The NB3N51054 is a precision, low phase noise clock generator that supports PCI Express requirements. The device accepts a 25 MHz fundamental mode parallel resonant crystal or a 25 MHz reference clock signal and generates four differential HCSL/LVDS outputs (See Figure 7 for LVDS interface) at 100 MHz clock frequency with maximum skew of 40 ps. Through I<sup>2</sup>C interface, NB3N51054 provides selectable spread spectrum options of -0.35% and -0.5% for applications demanding low Electromagnetic Interface (EMI) as well as optimum performance with no spread option. The I<sup>2</sup>C interface further enables control of each output and they can be enabled/ disabled individually.

## Features

- Uses 25 MHz Fundamental Crystal or Reference Clock Input
- Four Low Skew HCSL or LVDS Outputs
- I<sup>2</sup>C Support with Read Back Capability
- 04hTracospiofis of

# **BLOCK DIAGRAM**



## Table 1. PIN DESCRIPTION

Pin #	Pin Name	Туре	Description	
1	CLK2	HCSL or LVDS output	Noninverted clock output. (For LVDS levels see Figure 4)	
2	CLK2	HCSL or LVDS output	Inverted clock output. (For LVDS levels see Figure 4)	
3	GND	Ground	ower supply ground 0 V. This pin provides GND return path for the device.	
4	V <sub>DD</sub>	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.	
5	CLK1	HCSL or LVDS output	Noninverted clock output. (For LVDS levels see Figure 4)	
6	CLK1	HCSL or LVDS output	Inverted clock output. (For LVDS levels see Figure 4)	
7	CLK0	HCSL or LVDS output	Noninverted clock output. (For LVDS levels see Figure 4)	
8	CLKO	HCSL or LVDS output	Inverted clock output. (For LVDS levels see Figure 4)	
9	GND	Ground	Power supply ground 0 V. This pin provides GND return path for the device.	
10	V <sub>DD</sub>	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.	
11	GND	Ground	Power supply ground 0 V. This pin provides GND return path for the device.	
12	IREF	Output	Output current reference pin. Connect to precision resistor (typical 475 ) to set internal current reference	
13	GND	Ground	Power supply ground 0 V. This pin provides GND return path for the device.	
14	V <sub>DD</sub>	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.	
15	NC	NC	No Connect	
16	GND	Ground	Power supply ground 0 V. This pin provides GND return path for the device.	
17	V <sub>DD</sub>	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.	
18	XIN / CLKIN	Input	Crystal or Clock input. Connect to 25 MHz crystal OR 25 MHz single–ended reference clock input.	
19	XOUT	Input	Crystal input. Connect to 25 MHz crystal or float this pin while using reference clock.	
20	SCLK	Input	I <sup>2</sup> C compatible clock. Internal pull-up resistors	
21	SDATA	Input/ Output	I <sup>2</sup> C compatible data. Internal pull-up resistors	
22	V <sub>DD</sub>	Power	Positive supply voltage pin connected to +3.3 V typical supply voltage.	
23	CLK3	HCSL or LVDS output	Noninverted clock output. (For LVDS levels see Figure 4)	
24	CLK3	HCSL or LVDS output	Inverted clock output. (For LVDS levels see Figure 4)	

## **Recommended Crystal Parameters**

Crystal	Fundamental AT-Cut		
Frequency	25 MHz		
Load Capacitance	16–20 pF		
Shunt Capacitance, C0	7 pF Max		
Equivalent Series Resistance	50 Max		
Initial Accuracy at 25 °C	±20 ppm		
Temperature Stability	±30 ppm		
Aging	±20 ppm		

## **Serial Data Interface**

To enhance the flexibility and function of the clock synthesizer, a two-signal I<sup>2</sup>C serial interface is provided. All the clock outputs can be individually enabled or disabled in a glitch free manner though this serial data interface. In addition, spread spectrum can be enabled for -0.35% or -0.5% down spread or no spread option can be selected though this interface. The registers associated with the serial interface initialize to their default settings upon power-up.

## Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in Table 2 below.

## Table 2. COMMAND CODE DEFINITION

Bit	Description			
7	0 = Block read or Block write operation, 1= Byte read or byte write operation			
(6:0)	Byte offset for byte read or byte write operation. For Block read or Block write operations, these bits should be '0000000'.			

The block write and block read protocol is outlined in Table 3, while Table 4 outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

## Table 3. BLOCK READ AND BLOCK WRITE PROTOCOL

	Block Write Protocol		Block Read Protocol		
Bit	Description	Bit	Description		
1	Start	1	Start		
2:8	Slave address – 7 bits		Slave address – 7 bits		
9	Write = 0	9	Write = 0		
10	Acknowledge from slave	10	Acknowledge from slave		
11:18	11:18      Command code – 8 bit        '00000000' stands for block operation		Command code – 8 bit '00000000' stands for block operation		
19	Acknowledge from slave	19	Acknowledge from slave		
20:27	Byte count – 8 bits	20	Repeat start		
28	Acknowledge from slave	21:27	Slave address – 7 bits		
29:36	Data byte 0 – 8 bits	28	Read = 1		
37	Acknowledge from slave	29	Acknowledge from slave		
38:45	Data byte 1 – 8 bits	30:37	Byte count from slave – 8 bits		
46	Acknowledge from slave	38	Acknowledge from master		
			-		

## Table 4. BYTE READ AND BYTE WRITE PROTOCOL

Byte Write Protocol		Byte Read Protocol		
Bit	Description	Bit Description		
1	Start	1 Start		

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NB3N51054

## Table 13. ATTRIBUTES

Characteristi	Value	
Internal Pull-up Resistor (SCLK, SDAT	50 k	
ESD Protection Human Body Model		2 kV
Moisture Sensitivity, Indefinite Time Ou	t of Dray Pack (Note 1)	Level 1
Flammability Rating	UL 94 V–0 @ 0.125 in	
Transistor Count	132,000	
Meets or exceeds JEDEC Spec EIA/JE		

1. For additional information, see Application Note AND8003/D.

## Table 14. ABSOLUTE MAXIMUM RATING (Note 2)

Symbol	Parameter	Rating	Unit
V <sub>DD</sub>	Positive power supply with respect to GND	+4.6	V
VI	Input Voltage with respect to device GND	–0.5 V to V <sub>DD</sub> + 0.5 V	V
T <sub>A</sub>	Operating Temperature Range	-40 to +85	0

Table 16. AC ELECTRICAL CHARACTERISTICS (V\_{DD} = 3.3 V  $\pm$  5%, GND = 0 V, T\_A = -40°C to 85°C, Note 9)

# Table 17. AC ELECTRICAL CHARACTERISTICS – PCI EXPRESS JITTER SPECIFICATIONS

 $V_{DD}$  = 3.3 V  $\pm$  5%,  $T_A$  = –40°C to 85°C

Symbol	Parameter	Test Condition	Spread Condition	Min	Тур	Max	PCle Industry Spec	Unit
tj (PCIe Gen 1)	Cle Gen 1) Phase Jitter $f_{CLKIN} = 25$ MHz Crystal, Peak-to-Peak $f_{CLKOUT} = 100$ MHz	SSOFF		10	20	86	ps	
	(Notes 11 and 14)	Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2)	SSON (-0.5%)		19	28		
tREFCLK_HF_RMS (PCIe Gen 2)	Phase Jitter RMS (Notes 12 and 14)	f <sub>CLKIN</sub> = 25 MHz Crystal, f <sub>CLKOUT</sub> = 100 MHz	SSOFF		1.0	1.8	3.1	ps
		Input High Band: 1.5 MHz – Nyquist (clock frequency/2)	SSON (-0.5%)		1.1	1.9		
tREFCLK_LF_RMS (PCle Gen 2)	Phase Jitter RMS (Notes 12 and 14)	f <sub>CLKIN</sub> = 25 MHz Crystal, f <sub>CLKOUT</sub> = 100 MHz	SSOFF		0.1	0.15	3.0	ps
		Input Low Band: 10 kHz – 1.5 MHz	SSON (-0.5%)		0.8	1.1		
tREFCLK_RMS (PCIe Gen 3)	Phase Jitter RMS (Notes 13 and 14)	f <sub>CLKIN</sub> = 25 MHz Crystal,	SSOFF		0.35	0.7	1.0	ps
(FOIE Gen 3)		f <sub>CLKOUT</sub> = 100 MHz Input Evaluation Band: 0 Hz Nyquist (clock frequency/2)	SSON (-0.5%)		0.55	0.8		
tREFCLK_RMS (PCIe Gen 4)	Phase Jitter RMS (Notes 13 and 14)	f = 100 MHz, 25 MHz Crystal Input Evaluation Band: 0 Hz – Nyquist (clock frequency/2)	SSOFF		0.35	0.5	0.5	ps

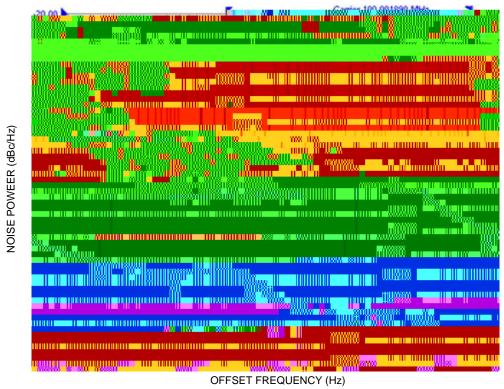
10. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

11. Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86 ps peak-to-peak for a sample size of 10<sup>6</sup> clock periods.

12. RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1 ps RMS for tREFCLK\_HF\_RMS (High Band) and 3.0 ps RMS for tREFCLK\_LF\_RMS (Low Band).

13. RMS jitter after applying system transfer function for the common clock architecture.

14. Measurement taken from differential output on single–ended channel terminated with R<sub>S</sub> = 33.2 , R<sub>L</sub> = 49.9 , with test load capacitance of 2 pF and current biasing resistor set at R<sub>REF</sub> = 475 . See Figure 6. This parameter is guaranteed by characterization. Not tested in production

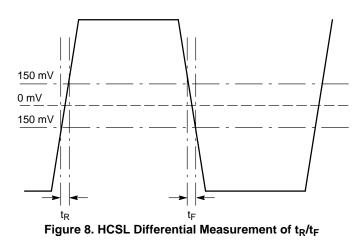


## PHASE NOISE

Figure 3. Typical Phase Noise Plot at 100 MHz ( $f_{CLKIN} = 25$  MHz Crystal ,  $f_{CLKOUT} = 100$  MHz, RMS Phase Jitter = 424 fs for Integration Range of 12 kHz to 20 MHz, Output Termination = HCSL type)

# **APPLICATION INFORMATION**

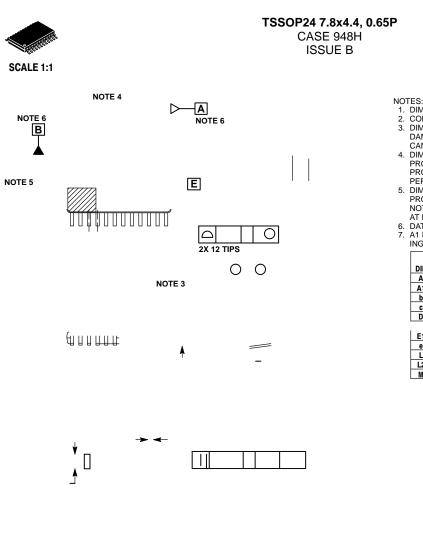
The outputs can be terminated to drive HCSL receiver (see Figure 6) or LVDS receiver (see Figure 7). HCSL output interface requires 49.9 termination resistors to GND for generating the output levels. LVDS output interface may not  $\begin{array}{ll} \mbox{require the } 100 & \mbox{near the LVDS receiver if the receiver has} \\ \mbox{internal } 100 & \mbox{termination. An optional series resistor } R_L \\ \mbox{may be connected to reduce the overshoots in case of} \end{array}$ 



## **ORDERING INFORMATION**

Device	Temperature	Package	Shipping <sup>†</sup>
NB3N51054DTR2G	–40°C to 85°C	TSSOP-24 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DATE 21 JUN 2012

- NOTES:
  DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  CONTROLLING DIMENSION: MILLIMETERS.
  DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
  DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D IS DETERMINED AT DATUM PLANE H.
  DIMENSION. INTERLEAD FLASH OR PROTRUSION. SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED
- NOT EXCEED 0.25 PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM PLANE H.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
  A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEAT-ING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS					
DIM	MIN MAX					
Α		1.20				
A1	0.Q5	0.15				
b	0.1	0.30				
C	0.ď	0,20				
D	7.70	7. 0				
E1	4.30	4.50				
е	0.65					

).50	0.75	
0.25		
0°	0	

GENERIC **MARKING DIAGRAM\*** 

<u>AAAAAAAAAAA</u>
XXXXX
XXXXG
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\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may

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