3.3 V, C a – 25 MH ,

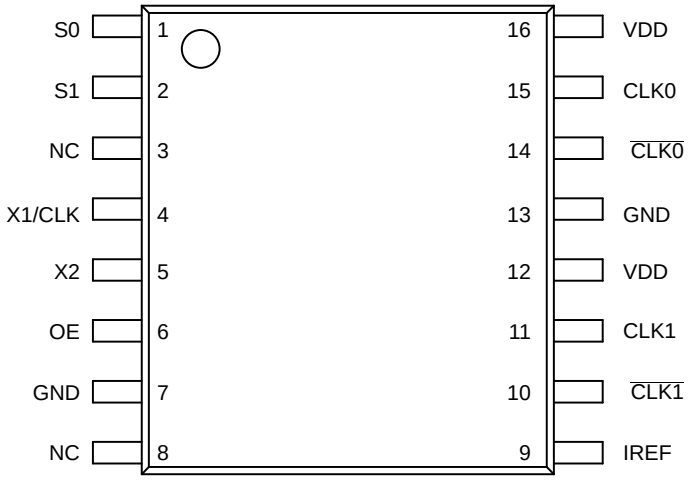


Figure 2. Pin Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Symbol	I/O	Description
1	S0	Input	LVTTL/LVCMOS frequency select input 0. Internal pullup resistor to V_{DD}. See output select table 2 for details.
2	S1	Input	LVTTL/LVCMOS frequency select input 1. Internal pullup resistor to V_{DD}. See output select Table 2 for details.
12, 16	V_{DD}	Power Supply	Positive supply voltage pins are connected to +3.3 V supply voltage.
4	X1/CLK	Input	Crystal or Clock input. Connect to 25 MHz crystal source or single−ended clock.
5	X2	Input	Crystal input. Connect to a 25 MHz crystal or leave unconnected for clock input.
6	OE	Input	Output enable tri−states output when connected to GND. Internal pullup resistor to V_{DD}.
7, 13	GND	Power Supply	Ground 0 V. These pins provide GND return path for the devices.
9	I_{REF}	Output	Output current reference pin. Precision resistor (typ. 475 Ω) is connected to set the output current.
11	CLK1	HCSL or LVDS Output	Noninverted clock output. (For LVDS levels see Figure 4)
10	$\overline{CLK1}$	HCSL or LVDS Output	Inverted clock output. (For LVDS levels see Figure 4)
15	CLK0	HCSL or LVDS Output	Noninverted clock output. (For LVDS levels see Figure 4)
14	$\overline{CLK0}$	HCSL or LVDS Output	Inverted clock output. (For LVDS levels see Figure 4)
3, 8	NC		Do not connect

Table 2. OUTPUT FREQUENCY SELECT TABLE WITH 25MHz CRYSTAL

S1*	S0*	CLK Multiplier	f_{CLKout} (MHz)
L	L	1x	25
L	H	4x	100
H	L	5x	125
H	H	8x	200

*Pins S1 and S0 default high when left open.

Recommended Crystal Parameters

Crystal	Fundamental AT−Cut
Frequency	25 MHz
Load Capacitance	16−20 pF
Shunt Capacitance, C0	7 pF Max
Equivalent Series Resistance	50 Ω Max
Initial Accuracy at 25 °C	±20 ppm
Temperature Stability	±30 ppm

Table 3. ATTRIBUTES

Characteristic		Value
ESD Protection	Human Body Model	> 2 kV
RPU − OE, S0 and S1 Pull−up Resistor		100 kΩ
Moisture Sensitivity, Indefinite Time Out of Dry Pack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	

Table 6. AC CHARACTERISTICS (V_{DD} = 3.3 V ±10%, GND = 0 V, T_A = −40°C to +85°C; Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{CLKIN}	Clock/Crystal Input Frequency		25		MHz
f_{CLKOUT}	Output Clock Frequency	25		200	MHz
θ_{NOISE}	Phase−Noise Performance f_{CLKx} = 200 MHz/100 MHz				dBc/Hz
	@ 100 Hz offset from carrier		−103/−109		
	@ 1 kHz offset from carrier		−118/−127.8		
	@ 10 kHz offset from carrier		−122/−136.2		
	@ 100 kHz offset from carrier		−130/−138.8		
	@ 1 MHz offset from carrier		−132/−138.2		
	@ 10 MHz offset from carrier		−149/−164		
t_{JITTER}	Period Jitter Peak−to−Peak (Note 6) f_{CLKx} = 200 MHz		10	20	ps
	Period Jitter RMS (Note 6) f_{CLKx} = 200 MHz		1.5	3	
	Cycle−Cycle RMS Jitter (Note 7) f_{CLKx} = 200 MHz		2	5	
	Cycle−to−Cycle Peak to Peak Jitter (Note 7) f_{CLKx} = 200 MHz		20	35	ps
$t_{JIT(\Phi)}$	Additive Phase RMS Jitter, Integration Range 12 kHz to 20 MHz		0.4		

Table 7. ELECTRICAL CHARACTERISTICS − PHASE JITTER PARAMETERS

Symbol	Parameter	Conditions (Notes 8 and 9)	Min	Typ	Max	Industry Limit	Unit
$t_{jphPCIeG1}$	RMS Phase Jitter	PCIe Gen 1 (Notes 10 and 11)		10	16	86	ps (p−p)
$t_{jphPCIeG2}$		PCIe Gen 2 Lo Band 10 kHz < f < 1.5 MHz (Note 10)		0.2	0.25	3	ps (rms)
		PCIe Gen 2 High Band 1.5 MHz < f < Nyquist (50 MHz) (Note 10)		0.9	1.2	3.1	ps (rms)
$t_{jphPCIeG3}$		PCIe Gen 3 (PLL BW of 2−4 MHz, CDR = 10 MHz) (Note 10)		0.2	0.3	1	ps (rms)
$t_{jphPCIeG4}$		PCIe Gen 4 (PLL BW of 2−4 MHz, CDR = 10 MHz) (Note 10)		0.21	0.3	0.5	ps (rms)
t_{jphUPI}		UPI (9.6 Gb/s, 10.4 Gb/s or 11.2 Gb/s, 100 MHz, 12 UI)		0.62	0.7	1.0	ps (rms)
t_{jphQPI_SMI}		QPI & SMI (100.00 MHz or 133.33 MHz, 4.8 Gb/s, 6.4 Gb/s 12UI) (Note 12)		0.1	0.3	0.5	ps (rms)
		QPI & SMI (100.00 MHz, 8.0 Gb/s, 12UI) (Note 12)		0.1	0.15	0.3	ps (rms)
		QPI & SMI (100.00 MHz, 9.6 Gb/s, 12UI) (Note 12)					

LVDS COMPATIBLE INTERFACE

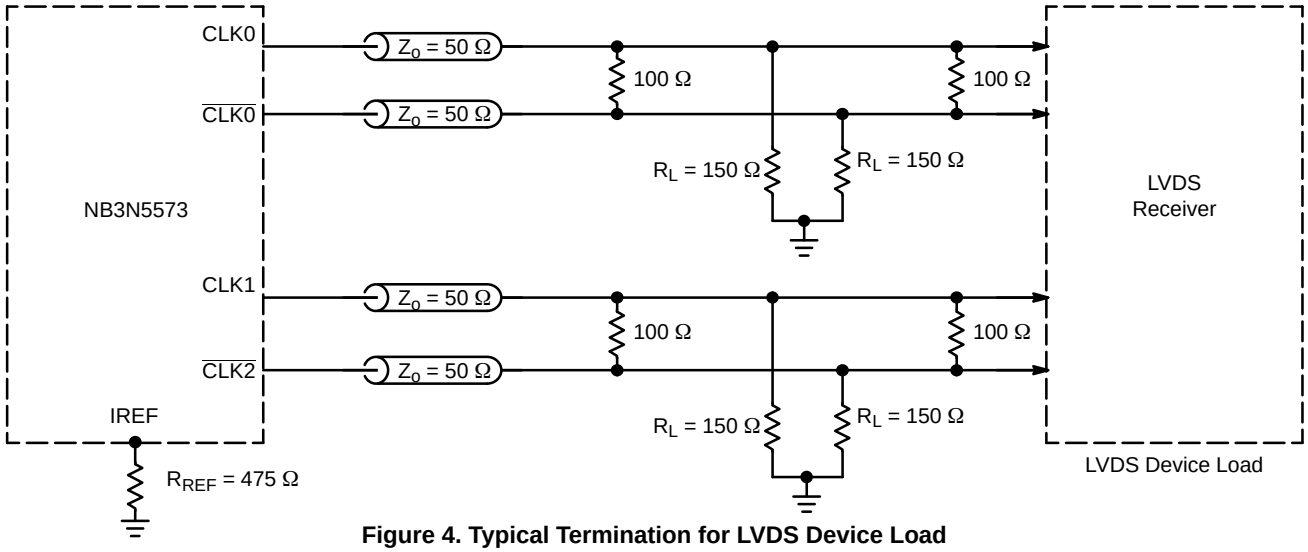
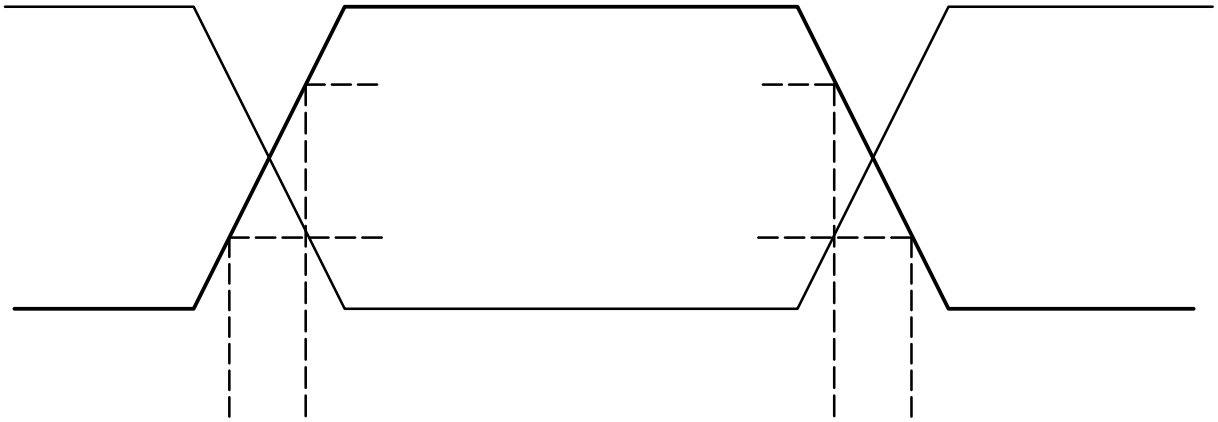
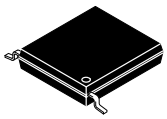


Figure 4. Typical Termination for LVDS Device Load





SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

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