



NB4L52

Table 2. PIN DESCRIPTION

| Pin | Name | I/O | Description |
|-----|-----------------------|------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------|
| 1 | V_{TD} | | Internal 50 Ω Termination Pin. (See Table 4) |
| 2 | D | ECL, CML, LVCMOS, LVDS, LVTTTL Input | Noninverted Differential Input. (Note 1) |
| 3 | \bar{D} | ECL, CML, LVCMOS, LVDS, LVTTTL Input | Inverted Differential Input. (Note 1) |
| 4 | $\overline{V_{TD}}$ | | Internal 50 Ω Termination Pin. (See Table 4) |
| 5 | V_{TCLK} | | Internal 50 Ω Termination Pin. (See Table 4) |
| 6 | CLK | ECL, CML, LVCMOS, LVDS, LVTTTL Input | Noninverted Differential Input. (Note 1) |
| 7 | \overline{CLK} | ECL, CML, LVCMOS, LVDS, LVTTTL Input | Inverted Differential Input. (Note 1) |
| 8 | $\overline{V_{TCLK}}$ | | Internal 50 Ω Termination Pin. (See Table 4) |
| 9 | V_{EE} | | Negative Supply Voltage |
| 10 | \bar{Q} | ECL Output | Inverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} 2.0 V. |
| 11 | Q | ECL Output | Noninverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} 2.0 V. |
| 12 | V_{CC} | | Positive Supply Voltage |
| 13 | V_{TR} | | Internal 50 Ω Termination Pin. (See Table 4) |
| 14 | R | L6.627 484.0441.896 .9071 refBTET128.523 468.26 Tc[2.0 V)92.1(.))JE L | |

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Table 4. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|----------|-----------------------|-------------|-------------|--------|------|
| V_{CC} | Positive Power Supply | V_{EE} | | | |

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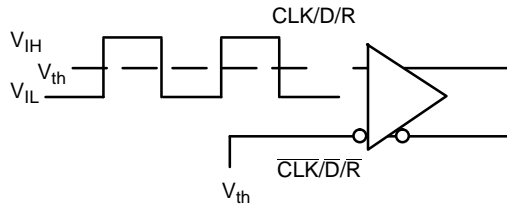


Figure 4. Differential Input Driven Single-Ended

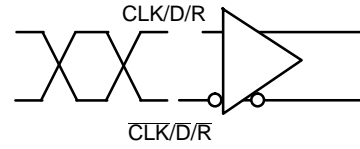


Figure 5. Differential Inputs Driven Differentially

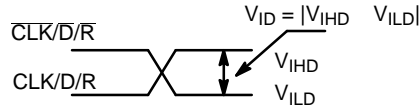


Figure 6. Differential Inputs Driven Differentially

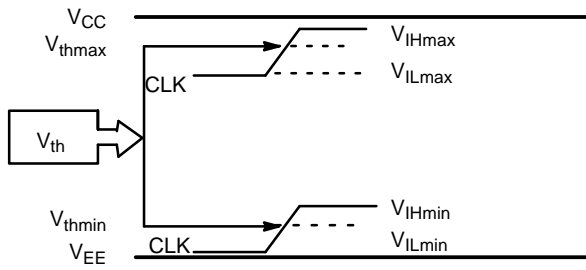


Figure 7. V_{th} Diagram

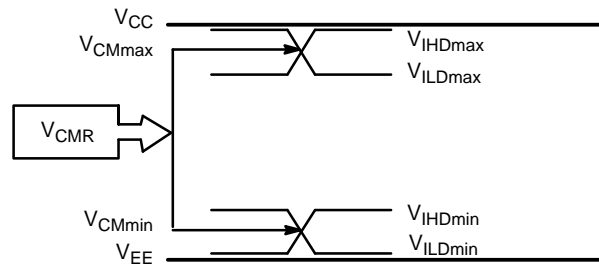
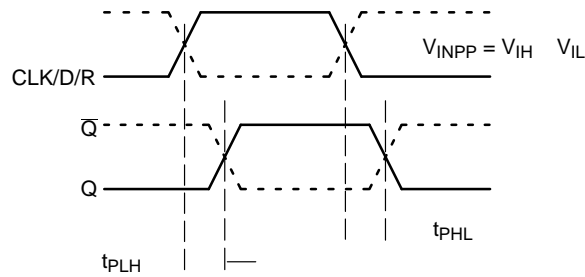
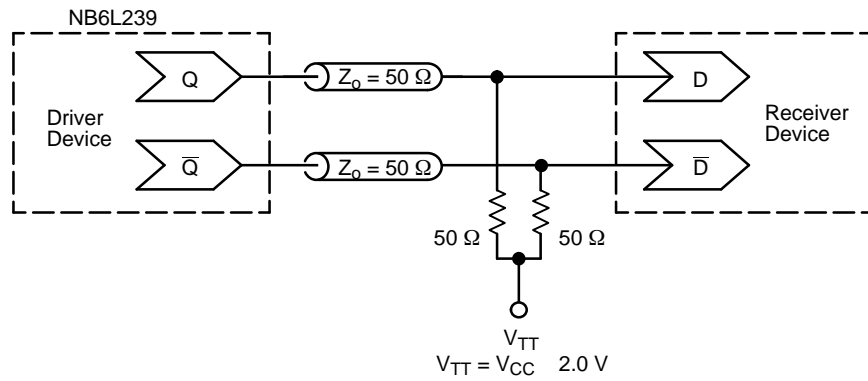


Figure 8. V_{CMR} Diagram



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**Figure 10. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------|-------------------------------|--------------------|
| NB4L52MNG | QFN 16, 3 x 3 mm (Pb Free) | 123 Units / Rail |
| NB4L52MNR2G | QFN 16, 3 x 3 mm (Pb Free) | 3000 / Tape & Reel |

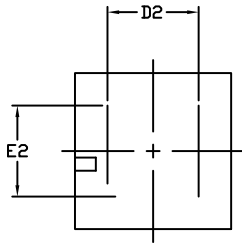
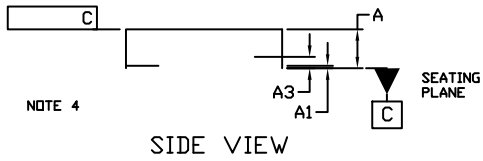
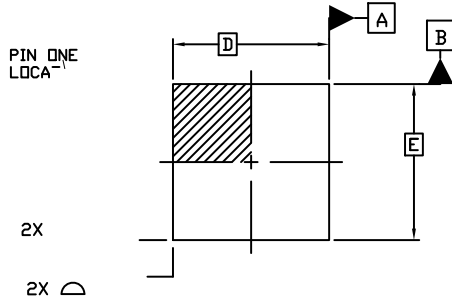
† For information on tape and reel specifications, see Application Note AND8020/D (Termination of ECL Logic Devices) or visit www.onsemi.com / Design 1 with Rev



1
SCALE 2:1

QFN16 3x3, 0.5P
CASE 485G
ISSUE G

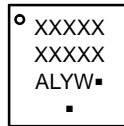
DATE 08 OCT 2021



BOTTOM VIEW

NOTE 3

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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