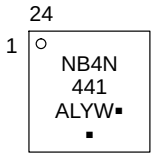
3.3 V Serial Input MultiProtocol PLL Clock Synthesizer, Differential LVPECL Output

NB4N441

QFN−24
MN SUFFIX
CASE 485L

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

Description

The NB4N441 is a precision clock synthesizer which generates a

PLL Lock Detect Output

- Output Enable
- Fully Integrated Phase Lock Loop with Internal Loop Filter
- Operating Range: V_{CC} = 3.135 V to 3.465 V
- Small Footprint 24 Pin QFN
- These Devices are Pb−Free and are RoHS Compliant

ORDERING INFORMATION

Device	Package	Shipping†
NB4N441MNG	QFN−24 (Pb−Free)	92 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB4N441

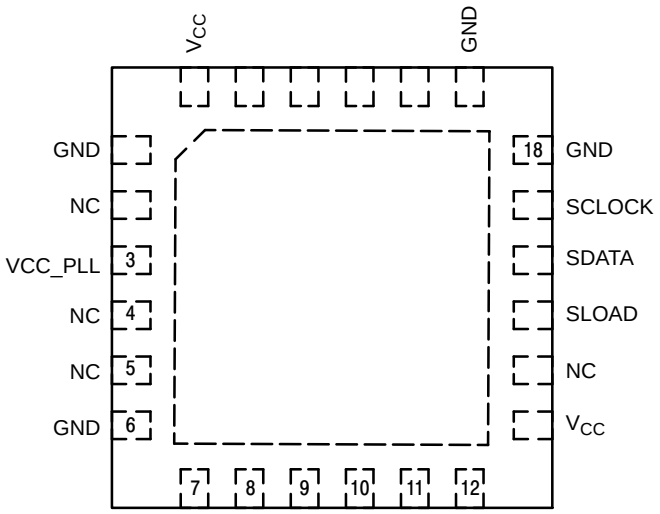


Figure 3. QFN−24 Lead Pinout (Top View)

Table 4. ATTRIBUTES

Characteristics	Value
Internal Input Pullup Resistor	37.5kΩ
Internal Input Pulldown Resistor	75kΩ
ESD Protection Human Body Model Machine Model	 > 1000 V > 150 V
Moisture Sensitivity (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V−0 @ 0.125 in
Transistor Count	2102

Table 6. DC CHARACTERISTICS V_{CC} = 3.135 V to 3.465 V, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic		Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Inputs and Outputs Loaded)		50	70	90	mA
I_{CCPLL}	PLL Power Supply Current		10	20	30	mA
V_{OH}	LVPECL Output HIGH Voltage (Notes 4 and 5) V_{CC} = 3.3 V		V_{CC} – 1145 2155	V_{CC} – 1030 2270	V_{CC} – 895 2405	mV
V_{OL}	LVPECL Output LOW Voltage (Notes 4 and 5) V_{CC} = 3.3 V		V_{CC} – 1945 1355	V_{CC} – 1760 1540	V_{CC} – 1695 1605	mV
V_{OHTTL}	Output HIGH Voltage ($\overline{\text{LOCKED}}$ Pin)	I_{OH} = −0.8 mA	2.5		V_{CC}	V
V_{OLTTL}	Output LOW Voltage ($\overline{\text{LOCKED}}$ Pin)		GND		0.4	V
V_{IH}	Input HIGH Voltage (LVTTL/LVCMOS)		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage (LVTTL/LVCMOS)		GND		0.8	V
I_{IH}	Input HIGH Current, OE SCLK, SDATA, SLOAD OE, SCLK, SDATA, SLOAD	V_{IN} = 2.7 V, VCC_{max} V_{IN} = 2.7 V, VCC_{max} V_{IN} = V_{CC}, VCC_{max}	6.0 20 20		26 60 60	μA μA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V, VCC_{max}			10	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. LVPECL Outputs loaded with 50 Ω termination resistors to V_{TT} = V_{CC} – 2.0 V for proper operation.
5. LVPECL Output parameters vary 1:1 with V_{CC}.

Table 7. AC CHARACTERISTICS V_{CC} = 3.135 V to 3.465 V, GND = 0 V, T_A = −40°C to +85°C (Note 6)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{IN}	Crystal Input Frequency External CLOCK Input Frequency (Pin 8) SCLOCK	10	27 27	28 50 10	MHz
V_{OUTPP}	Output Voltage Amplitude	600	800		mV
f_{VCO}	VCO Frequency Range	400		850	MHz
f_{CLKOUT}	Output Clock Frequency Range	12.5		425	MHz
t_R/t_{F_IN}	Input Clock Rise and Fall Time (CLK, Pin 8) (Note 7)			10	ns
t_{LOCK}	Maximum PLL Lock Time		0.5	5	ms
DCO	Output CLOCK Duty Cycle (Differential Configuration)	48		52	%
$t_{JITTER(pd)}$	Period Jitter (RMS, 1σ, 10,000 Cycles) (Notes 8 and 9)		3.5	6.5	ps
$t_{JITTER(pd)}$	Period Jitter (Peak−to−Peak, 10,000 Cycles) (Note 9)Peak, 10,000 Cycleak				

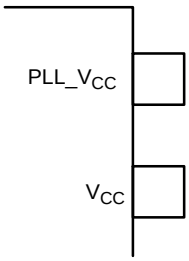


Figure 4. Power Supply Filter

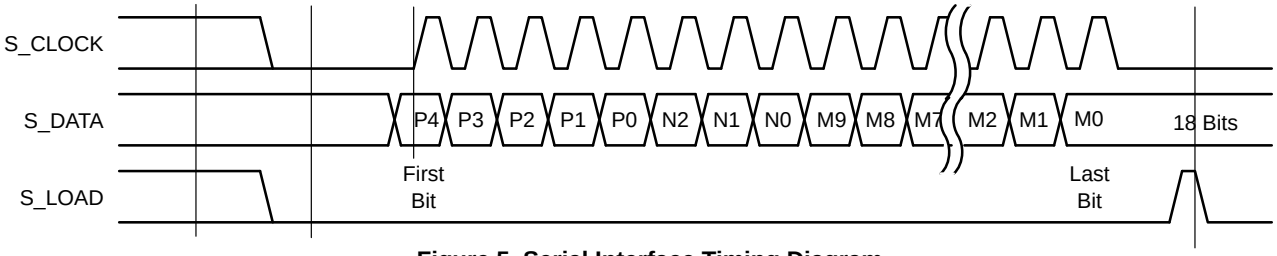


Figure 5. Serial Interface Timing Diagram

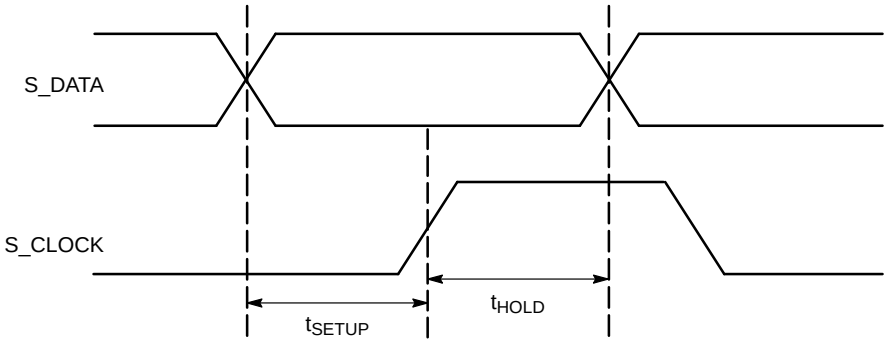


Figure 6. Setup and Hold

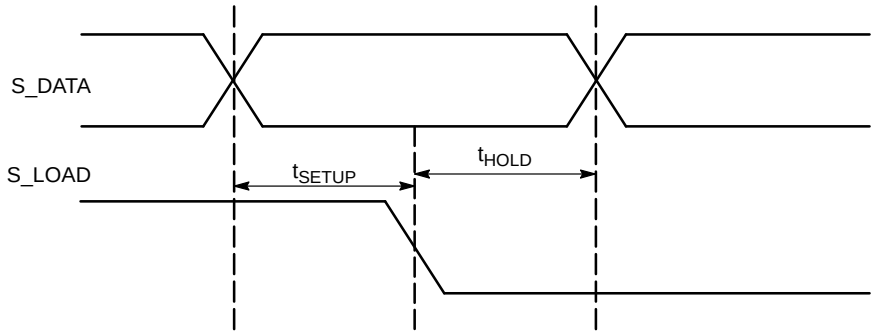


Figure 7. Setup and Hold

Jitter Performance

Jitter is a common parameter associated with clock generation and distribution. Clock jitter can be defined as the deviation in a clock's output transition from its ideal position.

– – (short term) is the period variation between two adjacent cycles over a defined number of observed cycles. The number of cycles observed is application dependent but the JEDEC specification is 1000 cycles.

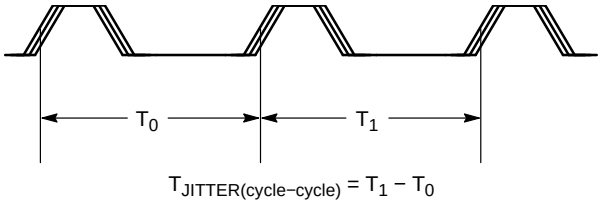


Figure 8. Cycle−to−Cycle Jitter

– – is the difference between the highest and lowest acquired value and is represented as the width of the Gaussian base.

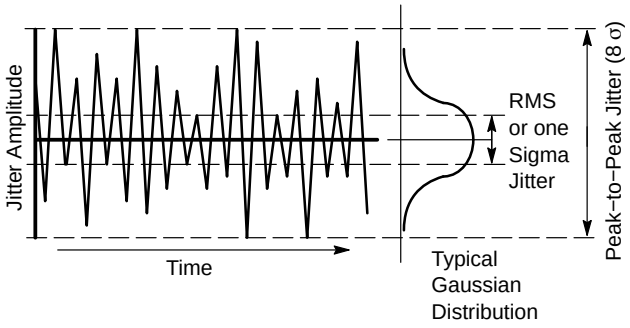


Figure 9. Peak−to−Peak Jitter

There are different ways to measure jitter and often they are confused with one another. The typical method of measuring jitter is to look at the timing signal with an oscilloscope and observe the variations in period to period or cycle to cycle. If the scope is set up to trigger on every rising or falling edge, set to infinite persistence mode and allowed to trace sufficient cycles, it is possible to determine the maximum and minimum periods of the timing signal. Digital scopes can accumulate a large number of cycles, create a histogram of the edge placements and record peak to peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. These scopes can also store a finite number of period durations and post processing software can analyze the data to find the maximum and minimum periods.

Recent hardware and software developments have resulted in advanced jitter measurement techniques. The Tektronix TDS series oscilloscopes have superb jitter analysis capabilities on non contiguous clocks with their histogram and statistics capabilities. The Tektronix TDSJIT2/3 Jitter Analysis software provides many key timing parameter measurements and will extend that capability by making jitter measurements on contiguous clock and data cycles from single shot acquisitions.

M1 by Amherst was used as well and both test methods correlated.

– is the maximum jitter observed at the end of a period's edge when compared to the position of the perfect reference clock's edge and is specified by the number of cycles over which the jitter is measured. The number of cycles used to look for the maximum jitter varies by application but the JEDEC spec is 10,000 observed cycles.

The NBC4N441 exhibit long term and cycle to cycle jitter, which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility associated with a synthesizer over a fixed frequency oscillator. The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

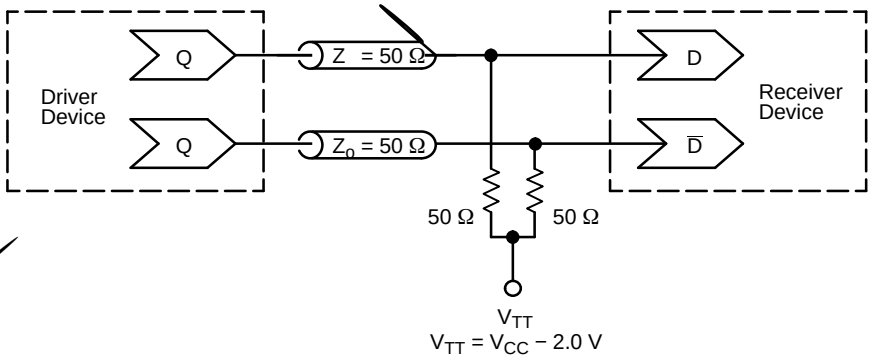


Figure 10. TTJTt5.16913Output Driver and Device Evaluation
(See Application Note AND8020/D −TJTt5.1of ECL Logic Devices.)

QFN24, 4x4, 0.5P
CASE 485L
ISSUE B

DATE 05 JUN 2012

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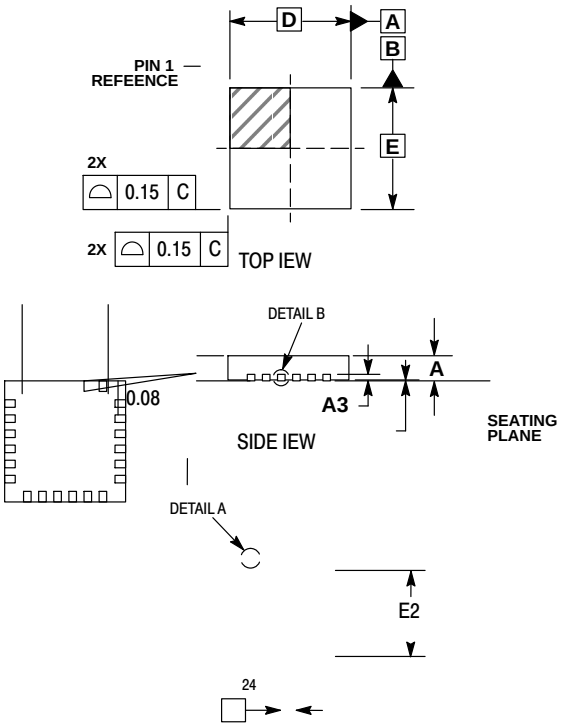
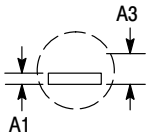
SCALE 2:1





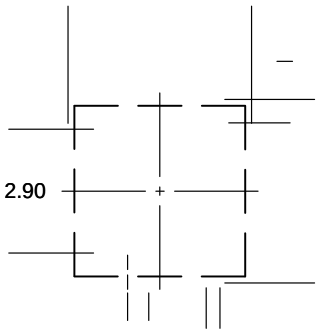
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

GENERIC
MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS