3.3 V/5 V, 50 MHz to 200 MHz PECL Clock Synthesizer

NB4N507A

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

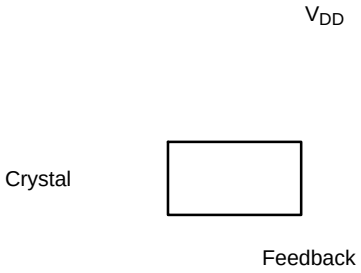


Figure 2. NB4N507A Logic Diagram

Table 3. PIN DESCRIPTION

Pin # SOIC−16	Name	I/O	Description
1	X1/CLK	Crystal Input	Crystal or Clock Input
2,3	V_{DD}	Power Supply	Positive Supply Voltage (3.0 V to 5.5 V)
4	S1	Tri−Level Input	Multiplier Select Pin; When Left Open, Defaults to V_{DD} ÷ 2
5,6	GND	Power Supply	Negative Supply Voltage
7,10,11,12, 15	NC	No Connect	Pin 10 does not require an external resistor. The NB4N507A will function with or without a resistor on Pin 10.
8	CLKOUT	PECL Output*	Non−inverted differential PECL clock output.
9	$\overline{\text{CLKOUT}}$	PECL Output*	Inverted differential PECL clock output.
13	OE	(LV)CMOS/(LV)TTL Input	Output Enable for the CLKOUT/$\overline{\text{CLKOUT}}$ Outputs. Outputs are enabled when HIGH or when left open; OE pin has internal pullup resistor. Disables both outputs when LOW. CLKOUT goes LOW, $\overline{\text{CLKOUT}}$ goes HIGH.
14	S0	Tri−Level Input	Multiplier Select Pin; When Left Open, Defaults to V_{DD} ÷ 2
16	X2	Crystal Input	Crystal Input

*The PECL Outputs are 15 mA open collector and must be DC loaded and AC terminated. See Figures 4, 5 and 6.

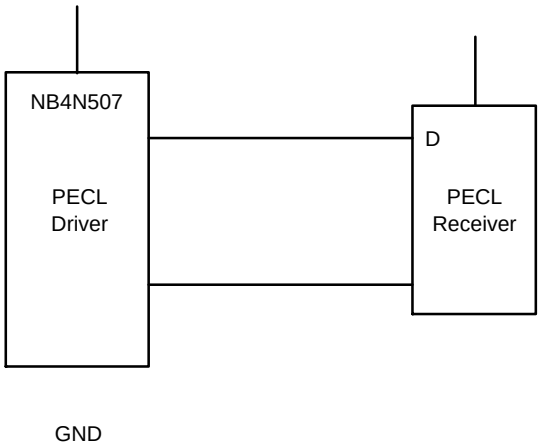
Table 4. ATTRIBUTES

Characteristics	Value
ESD Protection Human Body Model Machine Model Charged Device Model	> 1 kV > 150 V > 1 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count	1145 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		6	V
V_I	Input Voltage			GND − 0.5 ≤ V_I ≤ V_{DD} + 0.5	V
T_A	Operating Temperature Range				


NB4N507
PECL
Driver
D
PECL
Receiver
GND

APPLICATIONS INFORMATION

High Frequency Differential PECL Oscillators: The NB4N507A, along with a low frequency fundamental mode crystal, can build a high frequency differential PECL output oscillator. For example, a 10 MHz crystal connected to the NB4N507A with the 12X output selected (S1 = 0, S0 = 1) produces a 120 MHz PECL output clock.

Crystal Oscillator Input Interface

The NB4N507A features an integrated crystal oscillator to minimize system implementation costs. The oscillator circuit is a parallel resonant circuit and thus, for optimum performance, a parallel resonant crystal should be used.

As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the NB4N507A as possible to avoid any board level parasitics. Surface mount crystals are recommended, but not required.

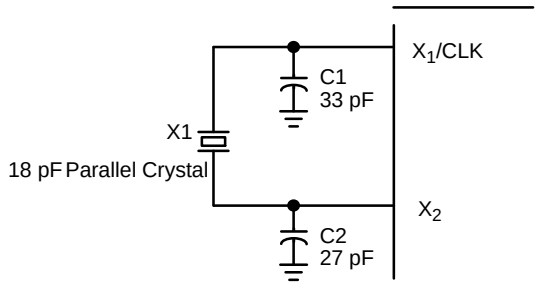


Figure 7. Crystal Input Interface

High Frequency VCXO: The bandwidth of the PLL is guaranteed to be greater than 10 kHz. This means that the PLL will track any modulation on the input with a frequency of less than 10 kHz. By using this property, a low frequency VCXO can be built. The output can then be multiplied by the NB4N507A, thereby producing a high frequency VCXO.

High Frequency TCXO: Extending the previous application, an inexpensive, low frequency TCXO can be built and the output frequency can be multiplied using the NB4N507A.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

ECLinPS is a trademark of

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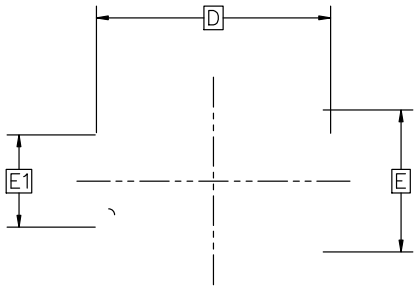
CASE 751B
ISSUE M

DATE 18 OCT 2024

3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.1[illegible]

nm TOTAL IN EXCESS OF THE

b DIMENSION AT MAXIMUM MATE



TOP VIEW

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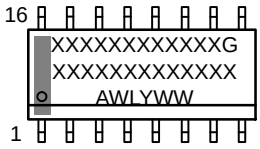
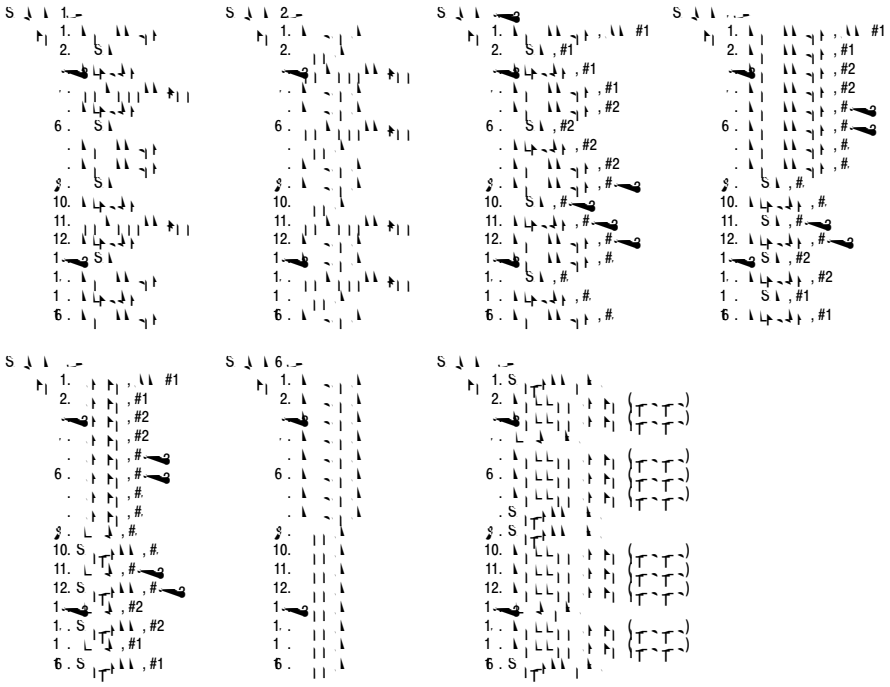
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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