2.5 V/ 3.3 V 2:1 n k/ V w p. p. s

Multi−Level Inputs w/ Internal Termination

N 6 56

The NB6L56 is a high performance Dual 2−to−1 Differential Clock or Data multiplexer. The differential inputs incorporate internal 50 termination resistors that are accessed through the VT pin. This feature allows the NB6L56 to accept various Differential logic level standards, such as LVPECL, CML or LVDS. Outputs are 800 mV

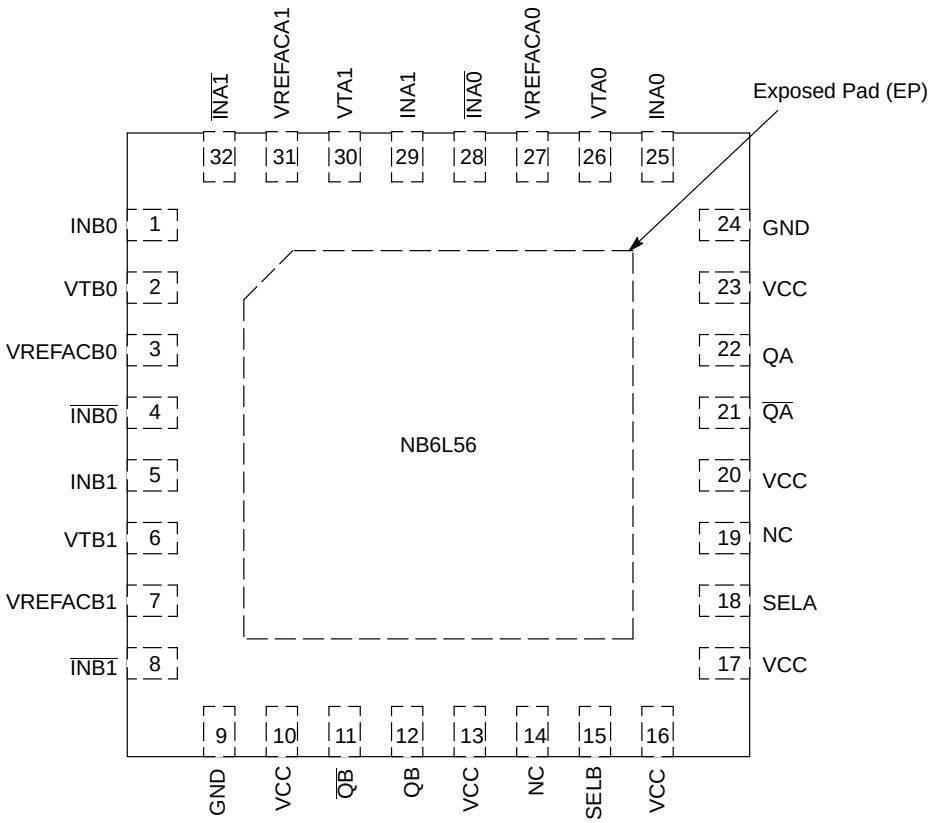


Figure 3. NB6L56 Pinout: QFN−32 (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Pin Description
1, 4 5, 8 25, 28 29, 32	INB0, $\overline{\text{INB0}}$ INB1, $\overline{\text{INB1}}$ INA0, $\overline{\text{INA0}}$ INA1, $\overline{\text{INA1}}$	LVPECL, CML, LVDS Input	Noninverted, Inverted Differential Input pairs (Note 1). Default state is indeterminate if left floating open. Do not connect unused input pairs with one input connected to VCC and the complementary input to GND. For differential and single ended interface, see “Interface Applications”.
2, 6 26, 30	VTB0, VTB1 VTA0, VTA1		Internal 100 Center−tapped Termination Pin for Differential Input pairs (Figure 4)
3 7 27 31	VREFACB0 VREFACB1 VREFACA0 VREFACA1	−	Output Voltage Reference for Capacitor−Coupled Inputs or Single Ended Interface (see “Interface Applications”)
15 18	SELB SELA	LVTTL / LVCMOS Input	Input Select pin; LOW for IN0 Inputs, HIGH for IN1 Inputs; defaults HIGH when left open

Table 2. INPUT SELECT FUNCTION TABLE

SELA/SELB	Q	$\overline{Q}$
L	INx0	$\overline{INx0}$
H	INx1	$\overline{INx1}$

Table 3. ATTRIBUTES

Characteristic		Value
ESD Protection	Human Body Model Machine Model	>2 kV 200 V
Input Pullup resistor (R_{PU})		75 k
Moisture Sensitivity (Note 3)	QFN32	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		1023
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 4)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		4.0	V
V_{INPP}	Differential Input Voltage |INx − $\overline{INx}$|			1.89	V
I_{IN}	Input Current Through RT (50 Resistor)			±40	mA
I_{OUT}	Output Current	Continuous Surge		±50 ±100	mA
I_{VREFAC}	VREFAC Sink/Source Current			±1.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
JA	Thermal Resistance (Junction−to−Ambient) (Note 4)	0 lfpm 500 lfpm	QFN − 32 QFN − 3231−to−Ambient)27(−65 to +150)TjET107.603 604.346		

Table 5. DC CHARACTERISTICS V_{CC} = 2.5 ± 5% (2.375 V to 2.625 V); V_{CC} = 3.3 ± 10% (3.0 V to 3.6 V) (Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Inputs and Outputs Open)		65	85	mA
LVPECL OUTPUTS					
V_{OH}	Output HIGH Voltage	V_{CC} – 1.145		V_{CC} – 0.895	mV
V_{OL}	Output LOW Voltage	V_{CC} – 2.000		V_{CC}	

Table 6. AC CHARACTERISTICS V_{CC} = 2.5 ± 5% (2.375 V to 2.625 V); V_{CC} = 3.3 ± 10% (3.0 V to 3.6 V) (Note 8)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{MAX}	Maximum Input Clock Frequency $V_{outpp} \geq 400$ mV Maximum Operating Data Rate (NRZ) $V_{outpp} \geq 400$ mV	2.5 2.5			Ghz Gbps
fSEL	Maximum Toggle Frequency, SELA/SELB	25	50		MHz
V_{OUTPP}	Output Voltage Amplitude (Differential Interconnect) $f_{in} \leq 2.5$ GHz	400			mVpp
t_{PLH}, t_{PHL}	Propagation Delay to Differential Outputs, @ 1 GHz, INxn/$\overline{INxn}$ to Qx, $\overline{Qx}$ SELx to Qx, $\overline{Qx}$	 160 100	 250 260	 360 400	ps
t_{PLH} Tempco	Differential Propagation Delay Temperature Coefficient		143		Δfs/°C
tskew	Input to Input per Bank Within Device Output Bank to Output Bank Within Device		10 12	20 25	ps
t_{JITTER}	DATA JITTER				ps

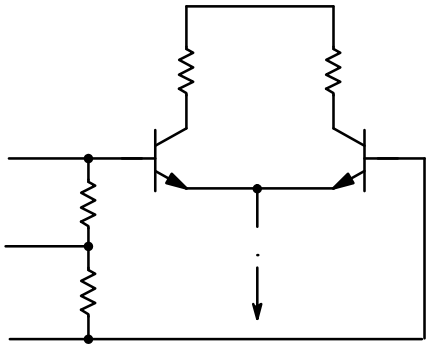


Figure 4. Simplified Input Structure

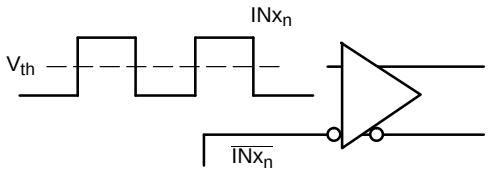


Figure 5. Differential Input Driven Single−Ended

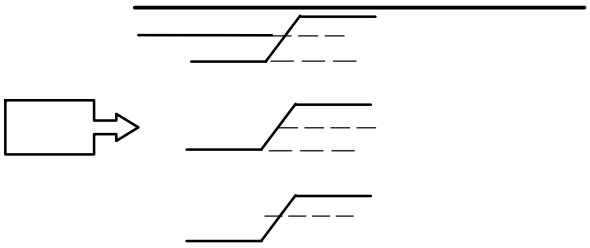


Figure 6. V_{th} Diagram

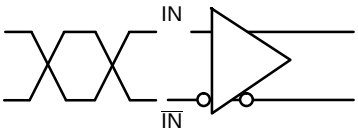


Figure 7. Differential Inputs Driven Differentially

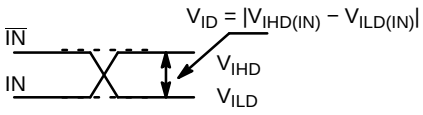


Figure 8. Differential Inputs Driven Differentially

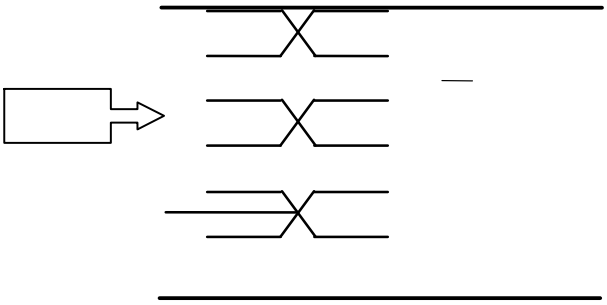


Figure 9. VCMR Diagram

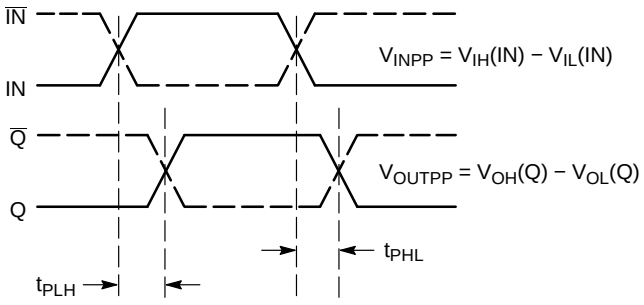


Figure 10. AC Reference Measurement

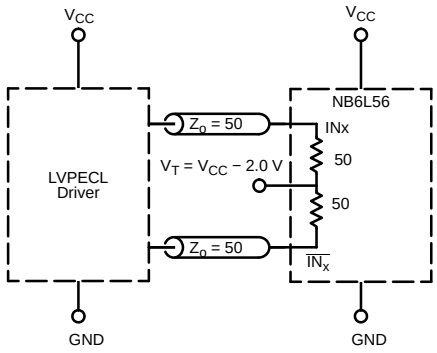


Figure 12. Typical LVPECL Interface (see AND8020)

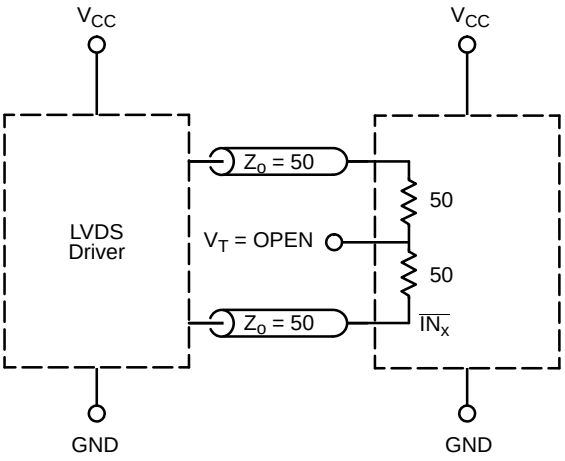


Figure 13. Typical LVDS Interface

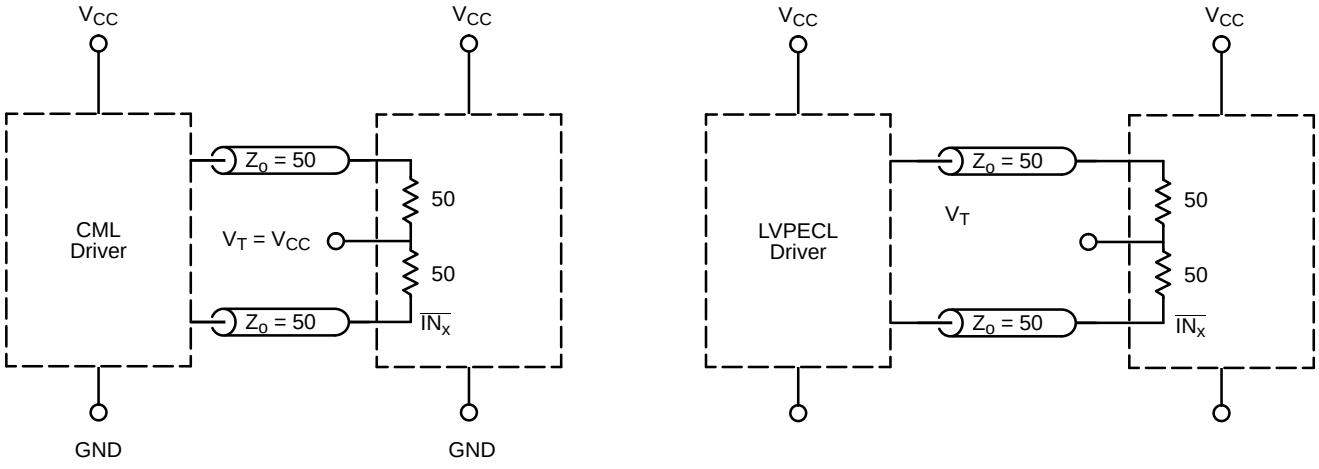


Figure 14. Typical Standard 50 Ω Load CML Interface

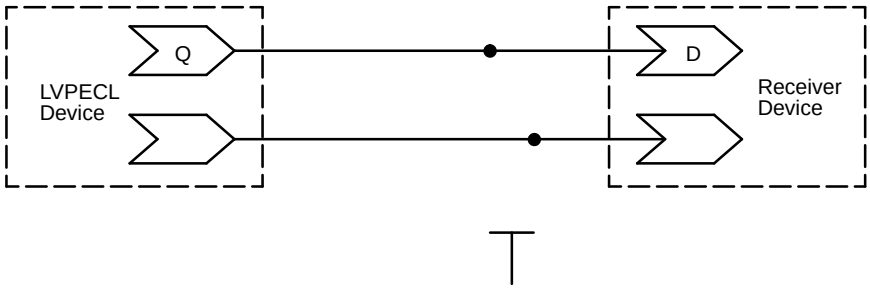
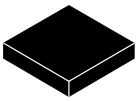


Figure 16. Typical Termination for LVPECL Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

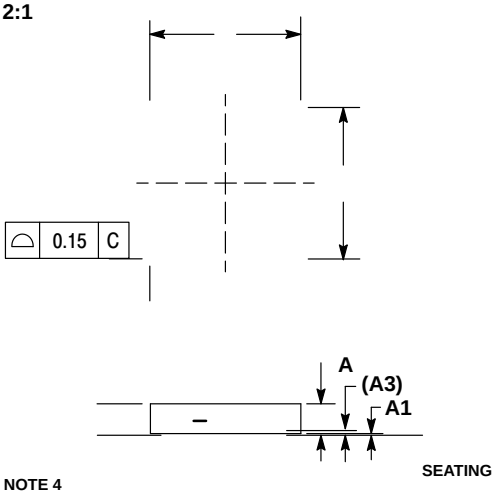
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

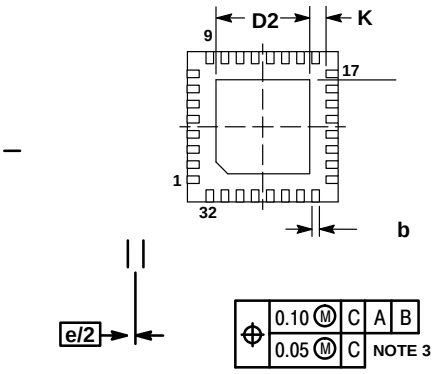
DATE 23 OCT 2013



SCALE 2:1

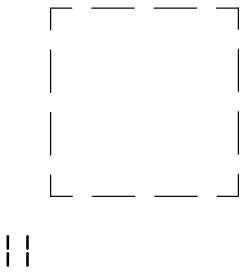


	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



XXXXXXXX
XXXXXXXX
AWLYYWW▪
▪Free indicator, “G” or

RECOMMENDED



PITCH

DIMENSION: MILLIMETERS

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