

2.5 /3.3 D 2 2
C
C L C /D
B /

Multi-Level Inputs w/ Internal Termination

B7L72

Description

The NB7L72M is a high bandwidth, low voltage, fully differential 2 x 2 crosspoint switch with CML outputs. The NB7L72M design is optimized for low skew and minimal jitter as it produces two identical copies of Clock or Data operating up to 7 GHz or 10 Gb/s, respectively. As such, the NB7L72M is ideal for SONET, GigE, Fiber Channel, Backplane and other clock/data distribution applications.

The differential IN/ \overline{IN} inputs incorporate internal 50 Ω termination resistors and will accept LVPECL, CML, or LVDS logic levels (see Figure 11). The 16 mA differential CML outputs provide matching internal 50 Ω terminations and produce 400 mV output swings when externally terminated with a 50 Ω resistor to V_{CC} (see Figure 9).

The NB7L72M is the 2.5 V/3.3 V version of the and NB7V72M and is offered in a low profile 3x3 mm 16-pin QFN package. Application notes, models, and support documentation are available at www.onsemi.com.

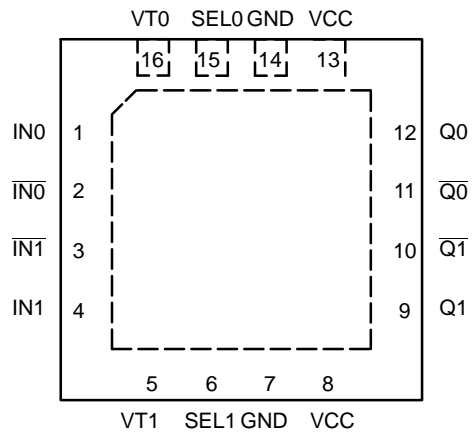
The NB7L72M is a member of the GigaComm™ family of high performance clock products.

A = Assembly Location
 L = Wafer Lot

Features

- Maximum Input Data Rate > 10 Gb/s
- Data Dependent Jitter < 10 ps pk-pk
- Maximum Input Clock Frequency > 7 GHz
- Random Clock Jitter < 0.5 ps RMS, Max
- 150 ps Typical Propagation Delay
- 30 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV peak-to-peak, typical
- Operating Range: $V_{CC} = 2.375$ V to 3.6 V with GND = 0 V
- Internal 50 Ω Input Termination Resistors
- QFN16 Package, 3mm x 3mm
- -40°C to +85°C Ambient Operating Temperature
- These are Pb-Free Devices

NB7L72M



NB7L72M

Table 3. ATTRIBUTES

Characteristics	Value
ESD Protection Human Body Model Machine Model	> 4 kV > 200 V
R _{PJ} – Input Pullup Resistor	75 kΩ
Moisture Sensitivity (Note 3) QFN16	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	212
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

3. For additional information, see Application Note [AND8003/D](#).

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	GND = 0 V		4.0	V
V _{IN}	Positive Input Voltage	GND = 0 V		-0.5 to V _{CC} +0.5	V
V _{INPP}	Differential Input Voltage I _N – I _N ̄			1.89	V
I _{IN}	Input Current Through R _T (50 Ω Resistor)			±40	mA
I _{OUT}	Output Current Through R _T (50 Ω Resistor)			±40	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient) (Note 4)	0 lfpm 500 lfpm	QFN16 QFN16	42 35	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case) (Note 4)		QFN16	4	°C/W
T _{sol}					

NB7L72M

Table 5. DC CHARACTERISTICS, Multi-Level Inputs $V_{CC} = 2.375\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ (Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
--------	----------------	-----	-----	-----	------

POWER SUPPLY CURRENT

V_{CC}	Power Supply Voltage	$V_{CC} = 2.5\text{ V}$ $V_{CC} = 3.3\text{ V}$	2.375 3.0	2.5 3.3	2.625 3.6	V
I_{CC}	Power Supply Current (Inputs and Outputs Open)		80	135	175	mA

CML OUTPUTS

V_{OH}	Output HIGH Voltage (Note 6)	$V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 40$ 3260 2460	$V_{CC} - 20$ 3280 2480	V_{CC} 3300 2500	mV
V_{OL}	Output LOW Voltage (Note 6)	$V_{CC} = 3.3\text{ V}$ $V_{CC} = 2.5\text{ V}$	$V_{CC} - 650$ 2650 $V_{CC} - 600$ 1900	$V_{CC} - 500$ 2800 $V_{CC} - 500$ 2000	$V_{CC} - 400$ 2900 $V_{CC} - 350$ 2150	mV

DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Note 7) (Figures 5 and 7)

V_{th}	Input Threshold Reference Voltage Range (Note 8)		1050		$V_{CC} - 100$	mV
V_{IH}	Single-Ended Input HIGH Voltage		$V_{th} + 100$		V_{CC}	mV
V_{IL}	Single-Ended Input LOW Voltage		GND		$V_{th} - 100$	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)		200		2800	mV

DIFFERENTIAL DATA/CLOCK INPUTS DRIVEN DIFFERENTIALLY (Figures 6 and 8) (Note 9)

V_{IHD}	Differential Input HIGH Voltage (IN_n, \overline{IN}_n)		1100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage (IN_n, \overline{IN}_n)		GND		$V_{CC} - 100$	mV
V_{ID}	Differential Input Voltage (IN_n, \overline{IN}_n) ($V_{IHD} - V_{ILD}$)		100		1200	mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 10) (Figure 9)		950		$V_{CC} - 50$	mV
I_{IH}	Input HIGH Current IN_n, \overline{IN}_n ($V_{TIN}/\overline{V_{TIN}}$ Open)		-150		150	μA
I_{IL}	Input LOW Current IN_n, \overline{IN}_n ($V_{TIN}/\overline{V_{TIN}}$ Open)		-150		150	μA

CONTROL INPUTS (SEL0, SEL1)

V_{IH}	Input HIGH Voltage for Control Pins		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage for Control Pins		GND		0.8	V
I_{IH}	Input HIGH Current		-150		150	μA
I_{IL}	Input LOW Current		-150		150	μA

TERMINATION RESISTORS

R_{TIN}	Internal Input Termination Resistor		40	50	60	Ω
R_{TOUT}	Internal Output Termination Resistor		40	50	60	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

5. Input and output parameters vary 1:1 with V_{CC} .

NB7L72M

Table 6. AC CHARACTERISTICS $V_{CC} = 2.375\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (Note 11)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{MAX}	Maximum Input Clock Frequency $V_{OUT} \geq 250\text{ mV}$ $V_{OUT} \geq 200\text{ mV}$	7.0 8.5			GHz
$f_{DATAMAX}$	Maximum Operating Data Rate (PRBS23)	10			Gbps
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) (See Figures 3 and 10, Note 12)	200	400		mV
t_{PLH} , t_{PHL}	Propagation Delay to Differential Outputs, @ 1GHz, Measured at Differential Cross-point $I_{Nn}/I_{N\bar{n}}$ to $Q_n/Q_{\bar{n}}$ SEL_n to $Q_n/Q_{\bar{n}}$	110	150	180	ps
$t_{PLH\ TC}$	Propagation Delay Temperature Coefficient		50		$\Delta fs/^\circ C$
t_{SKEW}	Output-to-Output Skew (within device) (Note 13) Device-to-Device Skew ($t_{pdmax} - t_{pdmin}$)			10 20	ps
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%) $f_{in} \leq 8.5\text{GHz}$	45	50	55	%
t_{jitter}	RJ – Output Random Jitter (Note 14) DJ – Deterministic Jitter (Note 15)		0.2	0.5 10	ps RMS ps pk-pk
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 16)	100		1200	mV
t_r , t_f	Output Rise/Fall Times @ 1 GHz (20% – 80%), Q, \bar{Q}	25	30	50	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

11. Measured using a 400 mV source, 50% duty cycle clock source. All output loading with external $50\ \Omega$ to V_{CC} . Input edge rates ≥ 40 ps (20% – 80%).
12. Output voltage swing is a single-ended measurement operating in differential mode.
13. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from cross-point of the inputs to the cross-point of the outputs.
14. Additive RMS jitter with 50% duty cycle clock signal.
15. Additive Peak-to-Peak data dependent jitter with input NRZ data at PRBS23.
16. Input voltage swing is a single-ended measurement operating in differential mode.

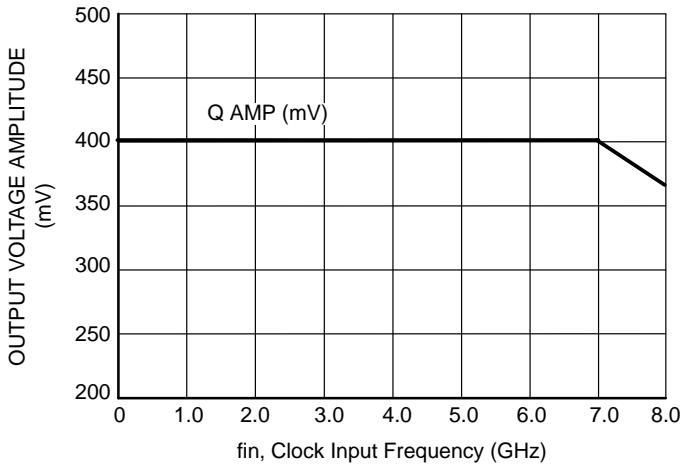


Figure 3. CLOCK Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typ)

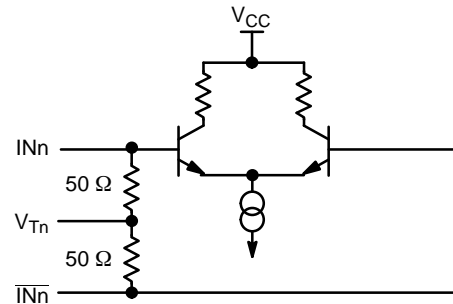


Figure 4. Input Structure

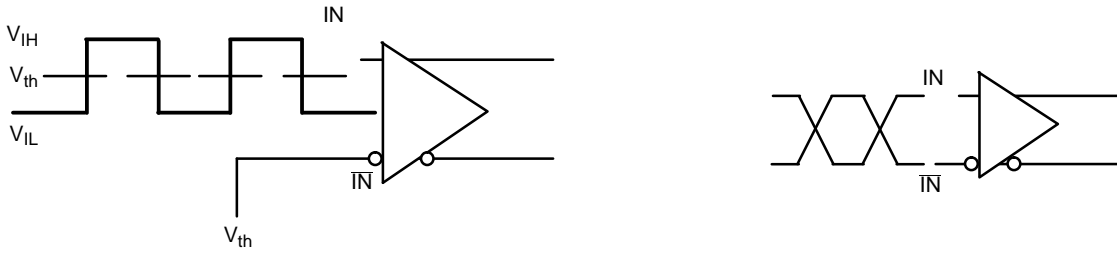
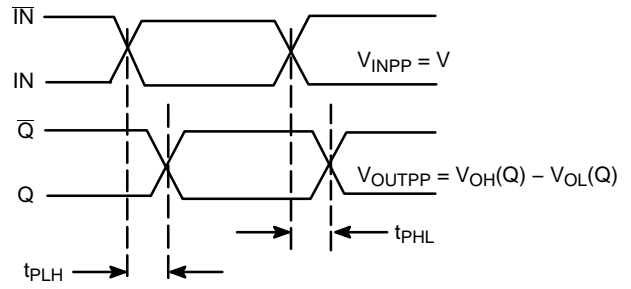
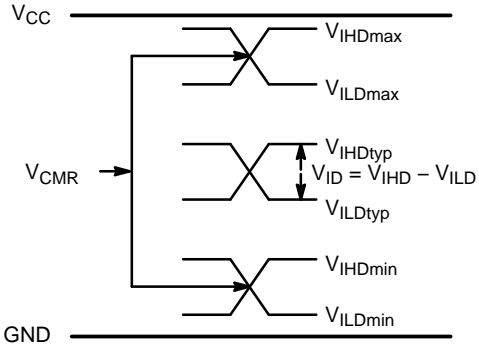
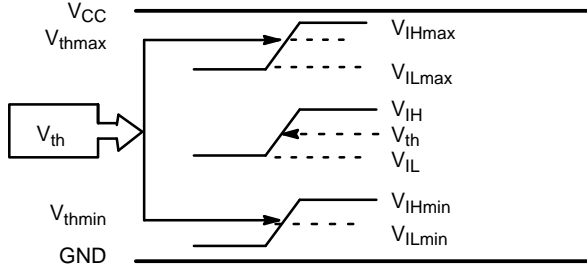


Figure 5. Differential Input Driven Single-Ended



NB7L72M

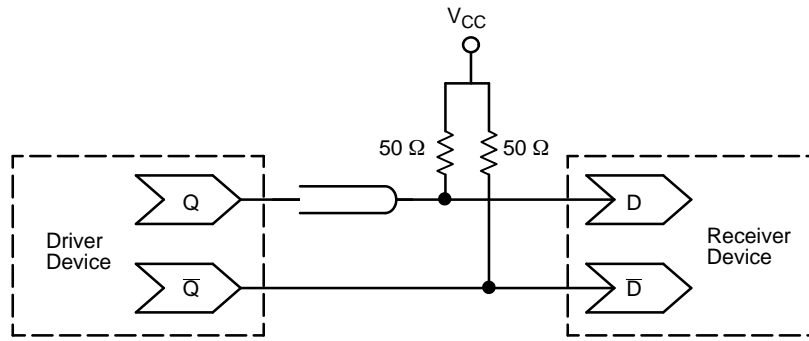


Figure 12. Typical Termination for CML Output Driver and Device Evaluation

NB7L72M

ORDERING INFORMATION

Device	Package	Shipping [†]
NB7L72MMNG	QFN16 (Pb-free)	123 Units / Tube
NB7L72MMNHTBG	QFN16 (Pb-free)	100 / Tape & Reel

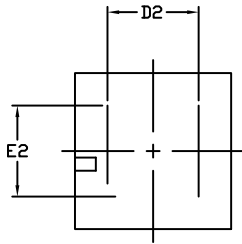
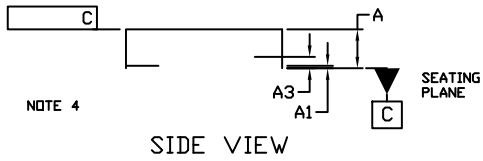
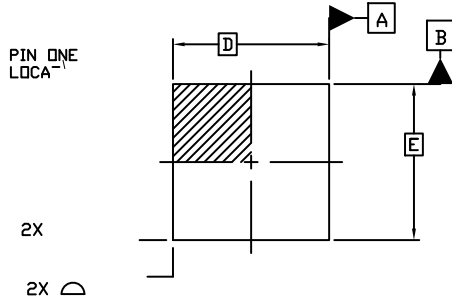
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



1
SCALE 2:1

QFN16 3x3, 0.5P
CASE 485G
ISSUE G

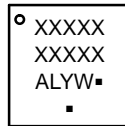
DATE 08 OCT 2021



NOTE 3

BOTTOM VIEW

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

onsemi, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**
