2.5 V/3.3 V SiGe Differential Smart Gate with Output Level Select

NB7L86A

The NB7L86A is a multi−function differential Logic Gate which can be configured as an AND/NAND, OR/NOR, XOR/XNOR, or 2:1 MUX. This device is part of the GigaComm™ family of high performance Silicon Germanium products. The device is housed in a 3 x 3 mm 16 pin QFN package.

Differential inputs incorporate internal 50 termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVCMOS/LVTTL, CML, or LVDS. The Output Level Select (OLS) input is used to program the peak−to−peak output amplitude between 0 and 800 mV in five discrete steps.

The NB7L86A employs input default circuitry so that under open input condition (Dx, $\overline{\text{Dx}}$, VTDx, $\overline{\text{VTDx}}$, VTSEL) the Outputs of the device remains stable.

Features

- Maximum Input Clock Frequency > 8 GHz Typical
- Maximum Input Data Rate > 8 Gb/s Typical
- 165 ps Typical Propagation Delay
- 40 ps Typical Rise and Fall Times
- Selectable Swing PECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- Selectable Swing NECL Output with NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.465 V
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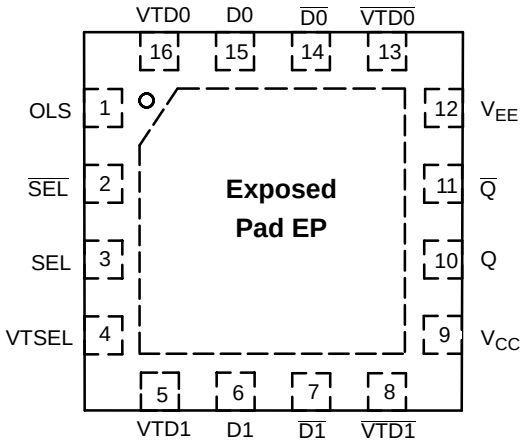


Figure 1. QFN16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	OLS (Note 3)	Input	Input for OLS (Output Level Select) Pin. Refer Table 2
2	$\overline{SEL}$	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input for Select Logic Pin, Single Ended or Inverted Differential
3	SEL	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input for Select Logic Pin, Single Ended or non−Inverted Differential
4	VTSEL (Note 1)		Pin with a common internal 50 termination from SEL/$\overline{SEL}$ Pins. Refer Table 7 for usage with different Interface options
5	VTD1 (Note 1)		Pin with an internal 50 termination from D1 Pin. Refer Table 7 for usage with different Interface options
6	D1	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input Pin, Non−inverted Differential or Single Ended with internal 75 k connected to V_{EE}
7	$\overline{D1}$	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input Pin, Inverted Differential or Single Ended with internal 75 k connected to V_{EE} and 36.5 k connected to V_{CC}
8	$\overline{VTD1}$ (Note 1)		Pin with an internal 50 termination from D1 Pin. Refer Table 7 for usage with different Interface options
9	V_{CC} (Note 2)		Positive Supply Voltage
10	Q	Output: Reduced Swing ECL	Output Pin, non−inverted Differential Output with typical 50 termination to $V_{TT} = V_{CC} - 2$ V
11	Q	Output: Reduced Swing ECL	Output Pin, inverted Differential Output with typical 50 termination to $V_{TT} = V_{CC} - 2$ V
12	V_{EE} (Note 2)		Negative Supply Voltage
13	$\overline{VTD0}$ (Note 1)		Pin with an internal 50 termination from D0 Pin. Refer Table 7 for usage with different Interface options
14	$\overline{D0}$	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input Pin, Inverted Differential or Single Ended with internal 75 k connected to V_{EE} and 36.5 k connected to V_{CC}
15	D0	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input Pin, Non−inverted Differential or Single Ended with internal 75 k connected to V_{EE}
16	VTD0 (Note 1)		Pin with an internal 50 termination from D0 Pin. Refer Table 7 for usage with different Interface options
	EP		Exposed Pad (EP) is thermally connected to the die for improved heat transfer out of the package. The exposed pad can be connected electrically to V_{EE} on the PCB board

1. In the differential configuration when the input termination pins (VTD0/1, $\overline{VTD0/1}$, VTSEL) are connected to a common termination voltage, or left open, and if no signal is applied then the device will be susceptible to self−oscillation.
2. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.
3. When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0$ V, 2 k resistor should be connected from OLS pin to V_{EE}.

Table 2. OUTPUT LEVEL SELECT OLS

OLS	Q/$\overline{Q}$ VPP	OLS Sensitivity
V_{CC}	800 mV	OLS − 75 mV
V_{CC} − 0.4 V	200 mV	OLS ± 150 mV
V_{CC} − 0.8 V	600 mV	OLS ± 100 mV
V_{CC} − 1.2 V	0 mV	OLS ± 75 mV
V_{EE} (Note 4)	400 mV	OLS ± 100 mV
Float	600 mV	N/A

4. When an output level of 400 mV is desired and V_{CC} − V_{EE} > 3.0 V, 2 k resistor should be connected from OLS to to V_{EE}.

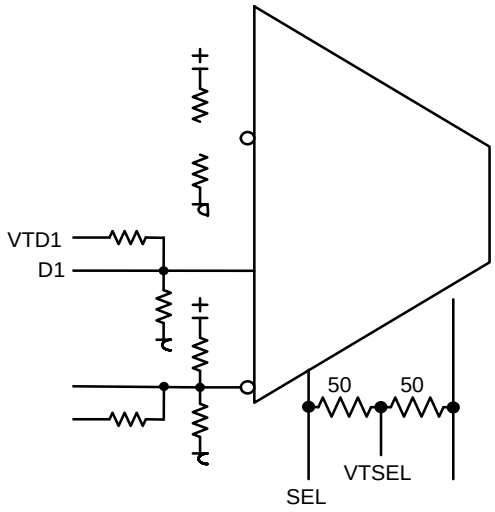


Table 7. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect $\overline{VTD0}$, VTD0, VTSEL, $\overline{VTD1}$, VTD1 TO V_{CC}

NB7L86A

Table 11. DC CHARACTERISTICS, INPUT WITH LVPECL OUTPUT V_{CC} = 3.3 V; V_{EE}

Table 12. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT

V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V, T_A = −40°C to +85°C (Note 21)

Symbol	Characteristics	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figure 12) (Note 25)											
V_{IHD}	Differential Input HIGH Voltage (D, $\overline{D}$, SEL, $\overline{SEL}$)	V_{EE}+ 1200		V_{CC}	V_{EE}+ 1200		V_{CC}	V_{EE}+ 120		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage (D, $\overline{D}$, SEL, $\overline{SEL}$)	V_{EE}		V_{CC}− 75	V_{EE}		V_{CC}− 75	V_{EE}		V_{CC}− 75	mV
V_{ID}	Differential Input Voltage (V_{IHD} – V_{ILD}) (D, $\overline{D}$, SEL, $\overline{SEL}$)	75		2600	75		2600	75		2600	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 26) (Figure 15)	V_{EE} + 1200		0	V_{EE} + 1200		0	V_{EE} + 1200		0	A
I_{IH}	(Input HIGH Current (@V_{IH}) D, $\overline{D}$,		30	100		30	100		30	100	A
	SEL, $\overline{SEL}$		5	50		5	50		5	50	
I_{IL}	(Input LOW Current (@V_{IL}) D, $\overline{D}$,		20	100		20	100		20	100	A
	SEL, $\overline{SEL}$		5	50		5	50		5	50	
TERMINATION RESISTORS											
R_{TIN}	Internal Input Termination Resistor	45									

Table 13. AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

Symbol	Characteristic		−40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Input Clock Frequency (See Figure 7) (Note 28)		7	8		7	8		7	8		GHz
V_{OUTPP}	Output Voltage Amplitude (OLS = V_{CC})	f_{in} < 7 GHz	590	730		470	720		540	700		mV
		f_{in} = 8 GHz	270	440		230	420		180	390		mV
t_{PLH} / t_{PHL}	Propagation Delay to Output Differential (Figure 15) D/SEL → Q		110	160	210	115	165	215	120	170	220	ps
t_{SKEW}	Duty Cycle Skew (Note 29)			5	15		5	15		5	15	ps
t_{SKEW}	Channel Skew	Q → D/SEL		5	20		5	20		5	20	ps
t_S	Set−Up Time (Dx to SEL)		30			30			30			ps
t_H	Hold−Up Time (Dx to SEL)		35			35			35			ps
t_{JITTER}	RMS Random Clock Jitter (See Figure 7) (Note 31) fin ≤ 7 GHz			0.5	1.5		0.5	1.5		0.5	1.5	ps
	Peak−to−Peak Data Dependent Jitter (Note 32) fin ≤ 7 Gb/s			12			12			12		
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 30)		75		1890	75		1890	75		1890	mV
t_r, t_f	Output Rise/ Fall Times	t_r	30	45	65	30	45	65	30	45	65	ps
	(20% − 80%) (Q, $\overline{Q}$) @ 1 GHz	t_f	17	35	65	17	35	65	17	35	65	

28. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 to V_{CC} − 2.0 V. Input edge rates 40 ps (20% − 80%).
29. t_{SKEW} = $|t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 15.
30. V_{INPP} (max) cannot exceed V_{CC} − V_{EE}.
31. Additive RMS jitter with 50% duty cycle clock signal at 7 GHz.
32. Additive Peak−

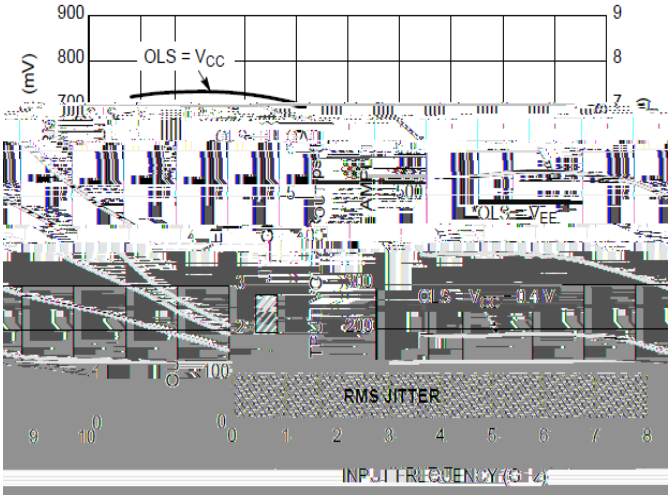


Figure 7. (V_{CC} − V_{EE} = 2.5 V @ 25°C)

Figure 8. (V_{CC} − V_{EE} = 3.3 V @ 25°C)

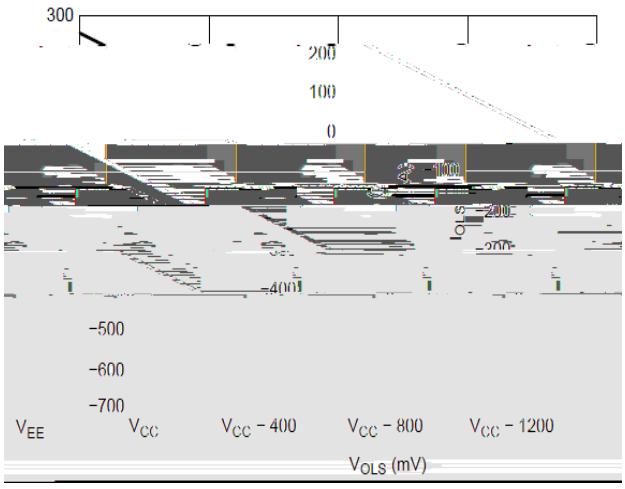


Figure 9. Typical OLS Input Current vs. OLS Input Voltage (V_{CC} − V_{EE} = 3.3 V @ 25°C)

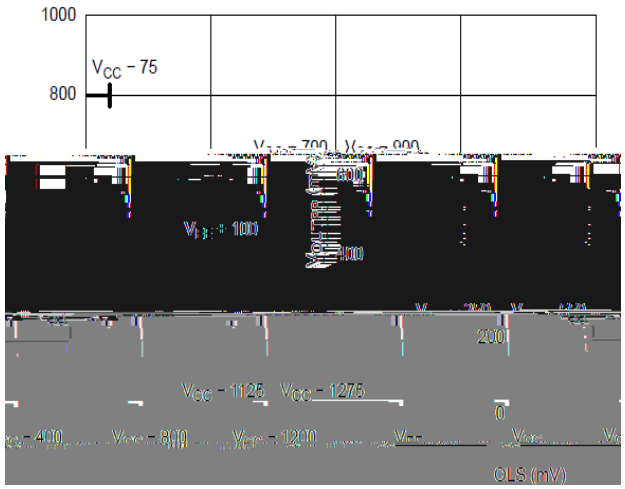


Figure 10. OLS Operating Area

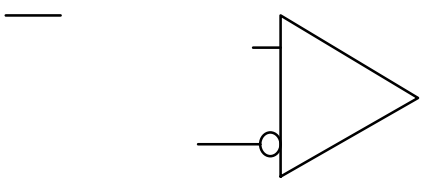


Figure 11. Differential Input Driven Single Ended

Figure 12. Differential Input Driven Differentially

NB7L86A

APPLICATION INFORMATION

All NB7L86A inputs can accept PECL, CML, LVTTL, LVCMOS and LVDS signal levels. The limitations for differential input signal (LVDS, PECL, or CML) are minimum input swing of 75 mV and the maximum input swing of 2500 mV. Within these conditions, the input voltage can range from V_{CC} to 1.2 V. Examples interfaces are illustrated below in a 50 environment (Z = 50). For output termination and interface, refer to application note AND8020/D.

THR

Table 14. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD and VTD to V_{CC} (refer Figure 18)
LVDS	Connect VTD and VTD together. (refer Figure 19)
AC−COUPLED	Bias VTD and VTD inputs within the Common Mode range (V_{CMR}) (refer Figure 20)
RSECL, PECL, NECL	Standard ECL termination techniques (refer Figure 21)
LVTTL, LVCMOS	An external voltage (V_{THR}) should be applied to the unused complementary differential input. Nominal V_{THR} is 1.5 V for LVTTL and V_{CC}/2 for LVCMOS inputs. This voltage must be within the V_{THR} specification (refer Figure 22)

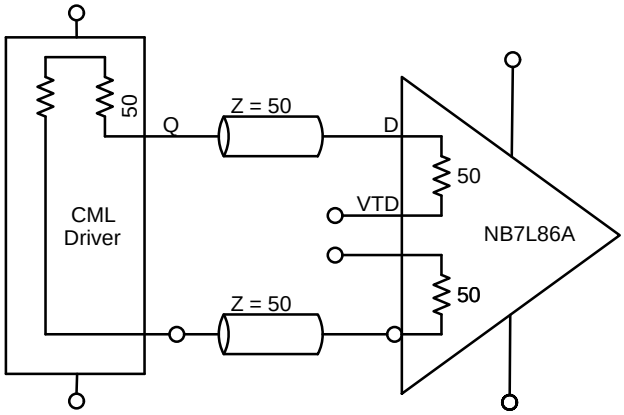


Figure 18. CML Interface

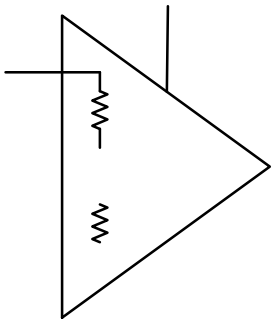
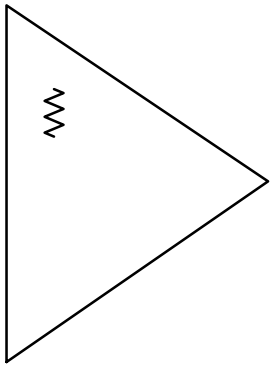


Figure 19. LVDS Interface



ORDERING INFORMATION

Device	Package Type	Shipping†
NB7L86AMNG	QFN16 (Pb−Free / Halide−Free)	123 Units / Rail
NB7L86AMNHTBG	QFN16 (Pb−Free / Halide−Free)	100 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

QFN16 3x3, 0.5P
CASE 485G
ISSUE G

DATE 08 OCT 2021

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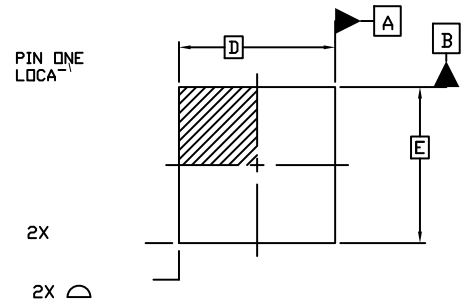
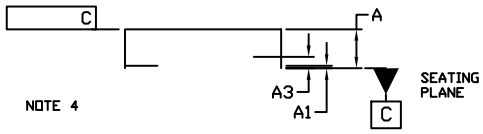
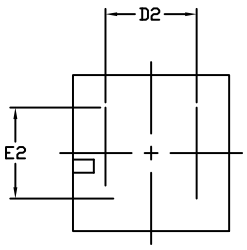
SCALE 2:1





SIDE VIEW



NOTE 3

BOTTOM VIEW

GENERIC
MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.