3.3 V USB 3.1 Gen-2 10 Gbps Dual Channel/ Single Port Linear Redriver

NB7NPQ1102M

Description

The NB7NPQ1102M is a high performance single−Port linear redriver designed for USB 3.1 Gen 1 and USB 3.1 Gen 2 applications that supports both 5 Gbps and 10 Gbps data rates. Signal integrity
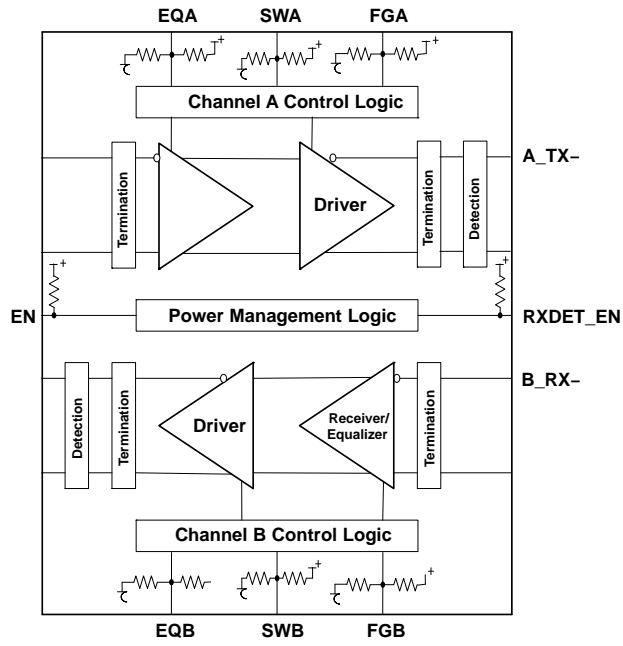
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Figure 1. Logic Diagram of NB7NPQ1102M

Table 2. OPERATING MODES

Modes	RIN	ROUT
Power Down Mode	67 kΩ to Ground	High Z
Unplug Mode	High Z	40 kΩ to V_{DD}
Low Power Slumber Mode	50 Ω to V_{DD}	40 kΩ to V_{DD}
Active Mode	50 Ω to V_{DD}	50 Ω to V_{DD}

Table 3. EQUALIZATION SETTINGS:

EQA/ EQB	EQ (dB)	
	@ 2.5 GHz	@ 5 GHz
Low "L" (Pin tied to Ground)	5.0	11.5
Rext "R" (68 kΩ tied from pin to Ground)	2.7	7.4
FLOAT "F" (Pin open)	4.0	9.9 (Default)
HIGH "H" (Pin tied to V_{DD})	6.5	13.1

Table 4. FLAT GAIN SETTING

FGA/ FGB	FG (dB)
Low "L" (Pin tied to Ground)	−1.2
Rext "R" (68 kΩ tied from pin to Ground)	0
FLOAT "F" (Pin open)	+1 .0 (Default)
HIGH "H" (Pin tied to V_{DD})	+2.0

Table 5. SWING SETTING

SWA/ SWB	SW (mVppd)
Low "L" (Pin tied to Ground)	800
Rext "R" (68 kΩ tied from pin to Ground)	1200
FLOAT "F" (Pin open)	1000 (Default)
HIGH "H" (Pin tied to V_{DD})	1100

Table 6. CHANNEL ENABLE SETTING

EN	Status
Low "0" (Pin tied to Ground)	Disabled
HIGH "1" (Pin tied to V_{DD})	Enabled (Default)

Table 7. RECEIVER DETECTION SETTING

RXDET_EN	Status
Low "0" (Pin tied to Ground)	Disabled
HIGH "1" (Pin tied to V_{DD})	Enabled (Default)

Table 8. ATTRIBUTES

Parameter		
ESD Protection	Human Body Model Charged Device Model	4 kV > 1.5 kV
Moisture Sensitivity, Indefinite Time Out of Dry pack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–O @ 0.125 in
Transistor Count		40517
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test		

1. For additional information, see Application Note AND8003/D.

Table 9. ABSOLUTE MAXIMUM RATINGS Over operating free–air temperature range (unless otherwise noted)

Parameter	Description	Min	Max	Unit
Supply Voltage (Note 2)	V_{DD}	−0.5	4.6	V
Voltage range at any input or output terminal	Differential I/O	−0.5	V_{DD} + 0.5	V
	LVCMOS inputs	−0.5	V_{DD} + 0.5	V
Output Current		−25	+25	mA
Power Dissipation, Continuous			1.0	W
Storage Temperature Range, T_{SG}		−65	150	°C
Maximum Junction Temperature, T_J			125	°C
Junction–to–Ambient Thermal Resistance @ 500 lfm, θ_{JA} (Note 3)			TBD	°C/W
Wave Solder, Pb–Free, T_{SOL}			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. All voltage values are with respect to the GND terminals.
3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 10. RECOMMENDED OPERATING CONDITIONS Over operating free−air temperature range (unless otherwise noted)

Parameter	Description		Min	Typ	Max	Unit
V_{DD}	Main power supply		3.0	3.3	3.6	V
T_A	Operating free−air temperature	Industrial Temperature Range	−40		+85	°C
C_{AC}	AC coupling capacitor		75	100	265	nF
Rext	External Resistor for input control setting "R", 5%			68		kΩ

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 11. POWER SUPPLY CHARACTERISTICS and LATENCY

Symbol	Parameter	Test Conditions	Min	Typ (Note 4)	Max	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
IDD_{Active}	Active mode current	EN = 1, 10 Gbps, compliance test pattern		115		mA
$IDD_{LPSlumber}$	Low Power Slumber mode current	EN = 1, no input signal longer than TLP−Slumber		0.4	0.64	mA
IDD_{Unplug}	Unplug mode current	EN = 1, no output load is detected		0.36	0.45	mA
IDDpd	Power−down mode current	EN = 0		10	50	μA
tpd	Latency	From Input to Output			2	ns

4. TYP values use V_{DD} = 3.3 V, T_A = 25°C

Table 12. CML RECEIVER AC/DC CHARACTERISTICS
V_{DD} = 3.3 V 0.3 V Over operating free−air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{RX−DIFF−DC}$	Differential Input Impedance (DC)		72	100	120	Ω
$R_{RX−SINGLE−DC}$	Single−ended Input Impedance (DC)	Measured with respect to GND over a voltage of 500 mV max.	18		30	Ω
$Z_{RX−HIZ−DC−PD}$	Common−mode input impedance for V>0 during reset or power−down (DC)	VCM = 0 to 500 mV	25			kΩ
$V_{RX−CM−AC−P}$	Common mode peak voltage	AC up to 5 GHz			150	mVpeak
$V_{RX−CM−DC−Active−Idle−Delta−P}$	Common mode peak voltage $\|AvgU0(\|V_{RX−D+}+V_{RX−D−}\|)/2 −AvgU1(\|V_{RX−D+}+V_{RX−D−}\|)/2\|$	Between U0 and U1. AC up to 5 GHz			200	mVpeak

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 13. LVCMOS CONTROL PIN CHARACTERISTICS
V_{DD} = 3.3 V 0.3 V Over operating free−air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
2−LEVEL CONTROL PINS LVCMOS INPUTS (EN, RXDET_EN)						
V_{IH}	DC Input Logic HIGH "1"		0.65 * V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	DC Input Logic LOW "0"		GND	GND	0.35 * V_{DD}	V
I_{IH}	High−level input current					

Table 14. TRANSMITTER AC/DC CHARACTERISTICS

V_{DD} = 3.3 V   0.3 V Over operating free−air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$V_{TX-DIFF-PP}$	Output differential p−p voltage swing at 100 MHz	Differential Swing				

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Table 14. TRANSMITTER AC/DC CHARACTERISTICS

V_{DD} = 3.3 V ± 0.3 V Over operating free−air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
CHANNEL PERFORMANCE						
V_{SW_5G}	−1 dB compression point output swing (5 GHz)	SWx = L SWx = R SWx = F SWx = H		600 900 750 825		mVppd
DDNEXT	Differential near−end crosstalk (Note 6)	100MHz to 5GHz, RXDET_EN = 1 Figure 3		−40		dB
SIGNAL AND FREQUENCY DETECTORS						
Vth_dsm	Low power slumber mode detector threshold	LFPS signal threshold in Low power Slumber mode	100		600	mVppd
Vth_am	Active mode detector threshold	Signal threshold in Active and Slumber mode (Note 8)	45		175	mVppd

6. Measured using a Vector Network Analyzer (VNA) with −15 dbm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50−Ω.
7. Guaranteed by design and characterization.
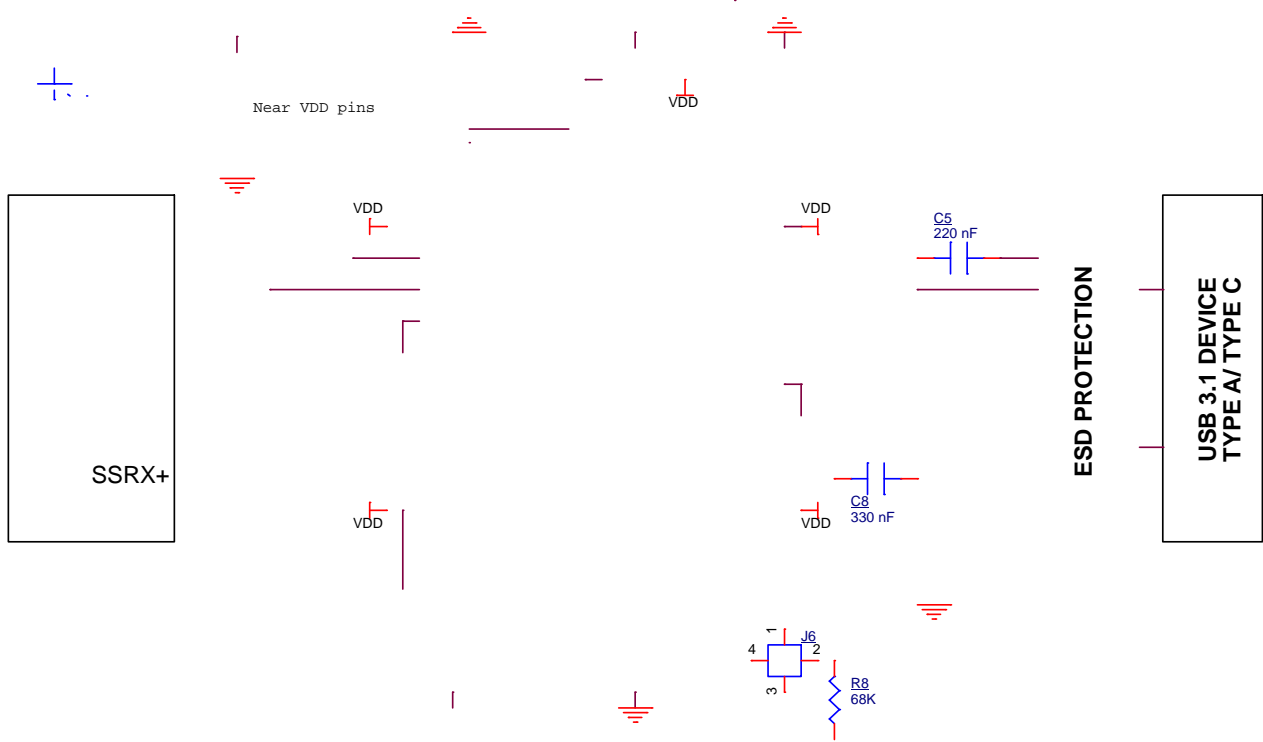8. Below the minimum is no signal @ 25°C. Above the maximum is active.
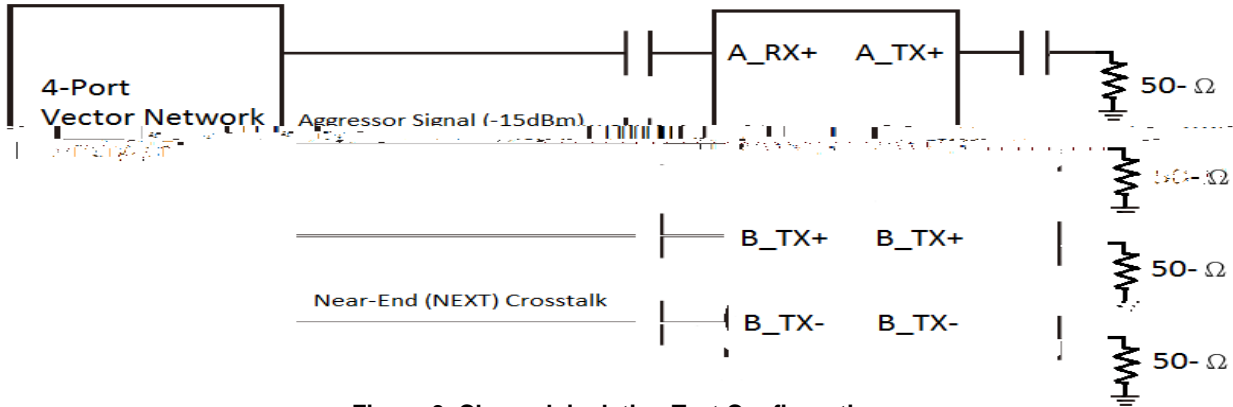
Figure 3. Channel−isolation Test Configuration

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Typical Application:

Near VDD pins

VDD

SSRX+

VDD

VDD

VDD

C5
220 nF

VDD

C8
330 nF

J6

R8
68K

ESD PROTECTION

USB 3.1 DEVICE
TYPE A/ TYPE C

WQFN30 2.50x4.50, 0.4P
CASE 510CK
ISSUE B

DATE 21 MAY 2020

A   = Assembly Location
L   = Wafer Lot
Y   = Year
W   = Work Week
▪   = Pb–Free Package

*This information is generic. Please refer to
 device data sheet for actual part marking.
 Pb–Free indicatorAing8orAing8orAi3Package-37.928 52.214 l0 52.214 l0 0 lSQ