

Description

The NB7NPQ1104M is a high performance 2–Port linear redriver designed for USB 3.1 Gen 1 and USB 3.1 Gen 2 applications that supports both 5 Gbps and 10 Gbps data rates. Signal integrity degrades from PCB traces, transmission cables, and inter–symbol interference (ISI). The NB7NPQ1104M compensates for these losses by engaging varying levels of equalization at the input receiver, and flat gain amplification on the output transmitter.

The NB7NPQ1104M offers programmable equalization and flat gain for each independent channel to optimize performance over various physical mediums.

The NB7NPQ1104M contains an automatic receiver detect function which will determine whether the output is active. The receiver detection loop will be active if the corresponding channel's signal detector is idle for a period of time. The channel will then move to Unplug Mode if a load is not detected, or it will return to Low Power Mode (Slumber mode) due to inactivity.

The NB7NPQ1104M comes in a 3.5 x 9 mm WQFN42 package and is specified to operate across the entire industrial temperature range, –40°C to 85°C.

Features

- $3.3 \text{ V} \pm 0.3 \text{ V}$ Power Supply
- 5 Gbps & 10 Gbps Serial Link with Linear Amplifier
- Device Supports USB 3.1 Gen 1 and USB 3.1 Gen 2 Data Rates
- Automatic Receiver Detection
- Integrated Input and Output Termination
- Pin Adjustable Receiver Equalization and Flat Gain
- 100–Ω Differential CML I/O's
- Auto Slumber Mode for Adaptive Power Management
- Hot–Plug Capable
- ESD Protection ±4 kV HBM
- Operating Temperature Range Industrial: -40°C to +85°C
- Package: WQFN42, 3.5 x 9 mm
- This is a Pb-Free Device

MARKING DIAGRAM



NB7N 1104 • AWLYYWWG

WQFN42 CASE 510AP

NB7N1104 = Specific Device Code

= Assembly Location

WL = Wafer Lot YY = Year WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping [†]

Typical Applications

- USB3.1 Type–A and Type–C Signal Routing
- Mobile Phone and Tablet
- Computer, Laptop and Notebook
- External Storage Device
- Docking Station and Dongle
- Active Cable, Back Planes
- Gaming Console, Smart T.V.

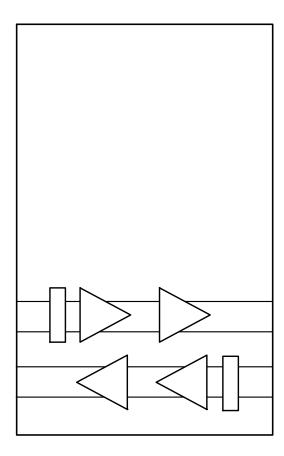


Figure 1. Logic Diagram of NB7NPQ1104M

Figure 2. WQFN-42 Package Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Туре	Description
1	FGA	INPUT	DC flat gain for channel A. 4–level input pin. Internal 100 k– Ω pull–up and 200 k– Ω pull–down.

Power Management

The NB7NPQ1104M has an adaptive power management feature in order to minimize power consumption. When the receiver signal detector is idle, the corresponding channel will change to low power slumber mode. Accordingly, both channels will move to low power slumber mode individually.

While in the low power slumber mode, the receiver signal detector will continue to monitor the input channel. If a channel is in low power slumber mode, the receiver detection loop will be active again. If a load is not detected, then the channel will move to Device Unplug Mode and continuously monitor for the load. When a load is detected, the channel will return to Low Power Slumber Mode and receiver detection will be active again per 6 ms.

Table 2. OPERATING MODES

Mode	R _{IN}	R _{OUT}
PD	67 k– Ω to GND	High-Z
Unplug Mode	High-Z	40 k– Ω to VDD
Low Power Slumber Mode	50–Ω to VDD	40 k– Ω to VDD
Active	50–Ω to VDD	50–Ω to VDD

Table 3. EQUALIZATION SETTING

EQ A/B/C/D are the selection pins for the equalization.

EQA/B/C/D	Equalizer Setting (dB)				
	@2.5 GHz	@5 GHz			
L (Tie 0– Ω to GND)	5.0	11.5			
R (Tie Rext to GND)	2.7	7.4			
F (Leave Open)	4.0	9.9 (Default)			
H (Tie 0– Ω to VDD)	6.5				

Table 11. CML RECEIVER AC/DC CHARACTERISTICS VDD = 3.3 V +/- 0.3 V Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
R _{RX-DIFF-DC}	Differential Input Impedance (DC)		72	100	120	Ω
R _{RX} -SINGLE-DC	Single-ended Input Impedance (DC)	Measured with respect to GND over a voltage of 500 mV max.	18		30	Ω
ZRX-HIZ-DC-PD	Common-mode input impedance for V>0 during reset or power-down (DC)	VCM = 0 to 500 mV	25			kΩ
Cac_coupling	AC coupling capacitance		75		265	nF
VRX-CM-AC-P	Common mode peak voltage	AC up to 5 GHz			150	mVpeak

VRX-CM-DC-Acti Common mode peak voltage ve-Idle-Delta-P |AvgU0(|V_{RX-D+}+V_{RX-D-}

	Parameter	Test Conditions	Min	Тур	Max	Unit
CHANNEL PERF	ORMANCE					
Gp	Peaking gain (Compensation at 5 GHz, relative to 100 MHz, 100 mVp–p sine wave input)	EQx = L				

PARAMETER MEASUREMENT DIAGRAMS

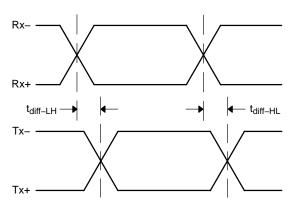


Figure 3. Propagation Delay

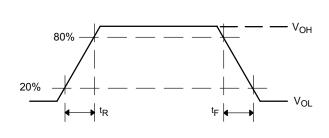


Figure 4. Output Rise and Fall Times

APPLICATION GUIDELINES

LFPS Compliance Testing

As part of USB 3.1 compliance test, the host or peripheral must transmit a LFPS signal that adheres to the spec parameters. The NB7NPQ1104M is tested as a part of a USB compliant system to ensure that it maintains compliance while increasing system performance.

LFPS Functionality

USB 3.1, Gen1 and Gen2 use Low Frequency Periodic Signaling.

(LFPS) to implement functions like exiting low-power modes, performing warm resets and providing link training between host and peripheral devices. LFPS signaling consists of bursts of frequencies ranging between 10 to 50 MHz and can have specific burst lengths or repeat rates.

Ping.LFPS for TX Compliance

During the transmitter compliance, the system under test must transmit certain compliance patterns as defined by the USB-IF. In order to toggle through these patterns for various tests, the receiver must receive a ping.LFPS signal from either the test suite or a separate pattern generator. The standard signal comprises of a single burst period of 100 ns at 20 MHz.

Control Pin Settings

Control pins A1, A0, B1, and B0 control the Flat Gain and the Equalization of channels A and B and control pins C1, C0, D1, and D0 control the Flat Gain and the Equalization of channels C and D of the NB7NPQ1104M Device.

The Float (Default) Setting "F" can be set by leaving the control pins in a floating state. The Redriver will internally

bias the control pins to the correct voltage to achieve this if the pin is not connected to a voltage source. The low Setting "L" is set by pulling the control pin to ground. Likewise the high setting "H" is set by pulling the pin high to VCC. The Rexternal setting can be set by adding a 68–K resistor from the control pin to ground. This will bias the Redriver internal voltage to 33% of VCC.

Linear Equalization

The linear equalization that the NB7NPQ1104M provides compensates for losses that occur naturally along board traces and cable lines. Linear Equalization boosts high frequencies and lower frequencies linearly so when transmitting at varying frequencies, the voltage amplitude will remain consistent. This compensation electrically counters losses and allows for longer traces to be possible when routing.

DC Flat Gain

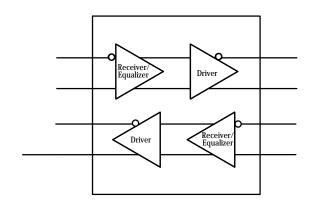
DC flat gain equally boosts high and low frequency signals, and is essential for countering low frequency losses.

DC flat gain can also be used to simulate a higher input signal from a USB Controller. If a USB controller can only provide 800 mV differential to a receiver, it can be boosted to 1128 mV using 2 dB of flat gain.

Total Gain

When using Flat Gain with Equalization in a USB application it is important to make sure that the total voltage does not exceed 1200 mV. Total gain can be calculated by adding the EQ gain to the FG.





USB 3.1 Receptacle

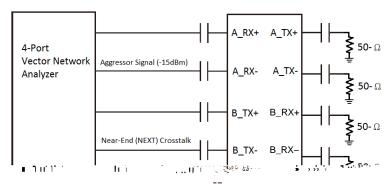
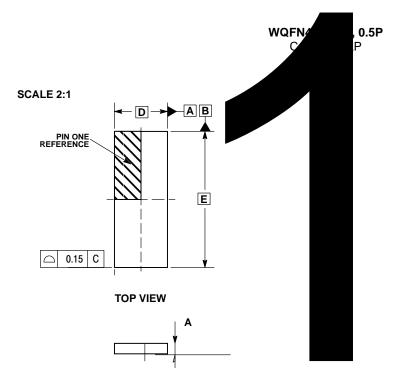


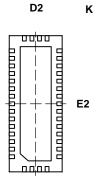
Figure 6. Channel-Isolation Test Configuration



DATE 15 FEB 2010

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION & APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

SIDE VIEW



BOTTOM VIEW

