



Figure 1. Logic Diagram of NB7NPQ1402E2M

Figure 2. UQFN24 Package Pinout (Top View)

Power Management

The NB7NPQ1402E2M has an adaptive power management feature in order to minimize power consumption. When the receiver signal detector is idle, the corresponding channel will change to low power slumber mode. Accordingly, both channels will move to low power slumber mode individually.

While in the low power slumber mode, the receiver signal detector will continue to monitor the input channel. If a channel is in low power slumber mode, the receiver detection loop will be active again. If a load is not detected, then the channel will move to Device Unplug Mode and continuously monitor for the load. When a load is detected, the channel will return to Low Power Slumber Mode and receiver detection will be active again per 6 ms.

Table 2. OPERATING MODES

Mode	R _{IN}	R _{OUT}
PD	67 k Ω to GND	High–Z
Unplug Mode	High–Z	40 k Ω to VDD
Low Power Slumber Mode	50 Ω to VDD	40 k Ω to VDD
Active	50 Ω to VDD	50 Ω to VDD

Table 3 SWING SETTING

SWA/B	SW (mVppd)
LOW "L" (Pin tied to Ground)	800
Rext "R" (68 k Ω tied from pin to Ground)	1200
Float "F" (Pin open)	1000 (Default)
HIGH "H" (Pin tied to VDD)	1100

Table 4. EQUALIZATION SETTING EQA/B are the selection pins for the equalization.

EQA/B	Equalizer Setting (dB)		
	@2.5 GHz	@5 GHz	
L (Tie 0– Ω to GND)	5.0	9.9	
R (Tie Rext to GND)	2.7	6.9	

F (Leave Open)

Table 9. ABSOLUTE MAXIMUM RATINGS Over operating free-air temperature range (unless otherwise noted)

Parameter	Description	Min	Max	Unit
Supply Voltage (Note 2)	Vdd	-0.5	4.6	V
Voltage range at any input or output terminal	Differential I/O	-0.5	V _{DD} + 0.5	V
	LVCMOS inputs	-0.5	V _{DD} + 0.5	V
Output Current		-25	+25	mA
			1.2	W
		-65	150	°C
			125	°C
			34	°C/W
			265	°C

ce. If any of these limits are exceeded, device functionality

2. All voltage values are with respect to the GND terminals.

3. JEDEC standard multilayer board - 2S2P (2 signal, 2 power).

Table 10. RECOMMENDED OPERATING CONDITIONS Over operating free-air temperature range (unless otherwise noted)

Parameter	Description		Тур	Max	Unit
V _{DD}	Main power supply	3.0	3.3	3.6	V
T _A	Operating free-air temperature Industrial Tempe	ature Range -40		+85	°C
C _{AC}	AC coupling capacitor	75	100	265	nF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 11. POWER SUPPLY CHARACTERISTICS and LATENCY

Symbol	Parameter	Test Conditions	Min	Typ (Note 4)	Max	Unit
VDD	Supply Voltage		3.0	3.3	3.6	V
IDD _{Active}	Active mode current	EN = 1, 10 Gbps, compliance test pattern		125	167	mA

Table 12. LVCMOS CONTROL PIN CHARACTERISTICS VDD = 3.3 V +/- 0.3 V Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit

4-Level Control Pins LVCMOS Inputs (EQA/B, FGA/B, SWA/B)

 V_{IR}

PARAMETER MEASUREMENT DIAGRAMS



Figure 3. Propagation Delay



Figure 4. Output Rise and Fall Times





Figure 6. Power Up Timing

Table 15. POWER UP TIMING

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Td_EN	VDD to Enable Assertion timing requirement	Figure 6.	0			ms
T_VCM	Stabilization time for VCM	Figure 6.		330	400	ms



Figure 7. Power Down Timing

Table 16. POWER DOWN TIMING

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Td_OFF	Delay time required from EN de-assertion until VDD is powered off	Figure 7.	900			ms

APPLICATION GUIDELINES

LFPS Compliance Testing

As part of USB 3.2 compliance test, the host or peripheral must transmit a LFPS signal that adheres to the spec parameters. The NB7NPQ1402E2M is tested as a part of a USB compliant system to ensure that it maintains compliance while increasing system performance.

LFPS Functionality

USB 3.2 Low Frequency Periodic Signaling.

(LFPS) to implement functions like exiting low-power modes, performing warm resets and providing link training between host and peripheral devices. LFPS signaling consists of bursts of frequencies ranging between 10 to 50 MHz and can have specific burst lengths or repeat rates.

Ping.LFPS for TX Compliance

During the transmitter compliance, the system under test must transmit certain compliance patterns as defined by the USB–IF. In order to toggle through these patterns for various tests, the receiver must receive a ping.LFPS signal from either the test suite or a separate pattern generator. The standard signal comprises of a single burst period of 100 ns at 20 MHz.

Control Pin Settings

Control pins SWA, FGA, EQA, SWB, FGB, and EQB control the Output Swing, Flat Gain and the Equalization of channels A and B of the NB7NPQ1402E2M Device.

The Float (Default) Setting "F" can be set by leaving the control pins in a floating state. The Redriver will internally bias the control pins to the correct voltage to achieve this if the pin is not connected to a voltage source. The low Setting "L" is set by pulling the control pin to ground. Likewise the high setting "H" is set by pulling the pin high to VCC. The Rexternal setting can be set by adding a 68 k Ω resistor from the control pin to ground. This will bias the Redriver internal voltage to 33% of VCC.

Linear Equalization

The linear equalization that the NB7NPQ1402E2M provides compensates for losses that occur naturally along board traces and cable lines. Linear Equalization boosts high frequencies and lower frequencies linearly so when transmitting at varying frequencies, the voltage amplitude will remain consistent. This compensation electrically counters losses and allows for longer traces to be possible when routing.

DC Flat Gain

DC flat gain equally boosts high and low frequency signals, and is essential for countering low frequency losses.

DC flat gain can also be used to simulate a higher input signal from a USB Controller. If a USB controller can only provide 800 mV differential to a receiver, it can be boosted to 1128 mV using 2 dB of flat gain.

Total Gain

When using Flat Gain with Equalization in a USB application it is important to make sure that the total voltage does not exceed 1200 mV. Total gain can be calculated by adding the EQ gain to the FG.

Typical Layout Practices

- RX and TX pairs should maintain as close to a 90 Ω differential impedance as possible.
- Limit the number of vias used on each data line. It is suggested that two or fewer are used.
- Traces should be routed as straight and symmetric as possible.
- RX and TX differential pairs should always be placed and routed on the same layer directly above a ground plane. This will help reduce EMI and noise on the data lines.
- Routing angles should be obtuse angles and kept to 135° or larger.
- To minimize crosstalk, TX and RX data lines should be kept away from other high speed signals.



Figure 8. Typical Application

Design Parameter	Value
Supply Voltage	3.3 V nominal, (3.0 V to 3.6 V)
Operation Mode (Control Pin Selection)	Floating by Default, adjust for application losses
TX AC Coupling Capacitors	220 nF nominal, 75 nF to 265 nF, see Figure 8
RX AC Coupling Capacitors	330 – 470 nF nominal, see Figure 8
Power Supply Capacitors	100 nF to GND close to each VCC pin, and 10 mF to GND on the VCC plane
Trace loss of FR4 before NB7NPQ1402E2M (Note 10)	Up to 11 dB Losses
Trace loss of FR4 after NB7NPQ1402E2M (Note 10)	Up To 3 dB Losses. Keep as short as possible for best performance.
Linear Range at 5 GHz	900 mV differential
DC Flat Gain Options	-1.2 dB, -0.2 dB, +0.8 dB, +1.8 dB
Equalization Options	6.9 to 12.1 dB
Differential Trace Impedance	90 Ω ±10%

Table 17. DESIGN REQUIREMENTS

10. Trace loss of FR4 was estimated to have 1 dB of loss per 1 inch of FR4 length with matched impedance and no VIAS.

UQFN24 2.5x2.5, 0.35P CASE 523AB ISSUE A

DATE 20 AUG 2021



XXXX = Specific Device Code A = Assembly Location

- = Wafer Lot
- L

I

- Υ = Year
- W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-

onsemi, NSC '., and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at <u>www.onsemi.com/site/pdf/Patent-Marking.pdf</u>. onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using data sheets and/or specifications can and do vary in different applications and actual performance may

gypicals'must be validated for each customer application by customechatical eperts. onsemi does not convey any license ights of others. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems ices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should h unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal ture is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: <u>www.onsemi.com/design/resources/technical-documentation</u> onsemi Website: <u>www.onsemi.com</u> ONLINE SUPPORT: <u>www.onsemi.com/support</u> For additional information, please contact your local Sales Representative at <u>www.onsemi.com/support/sales</u>