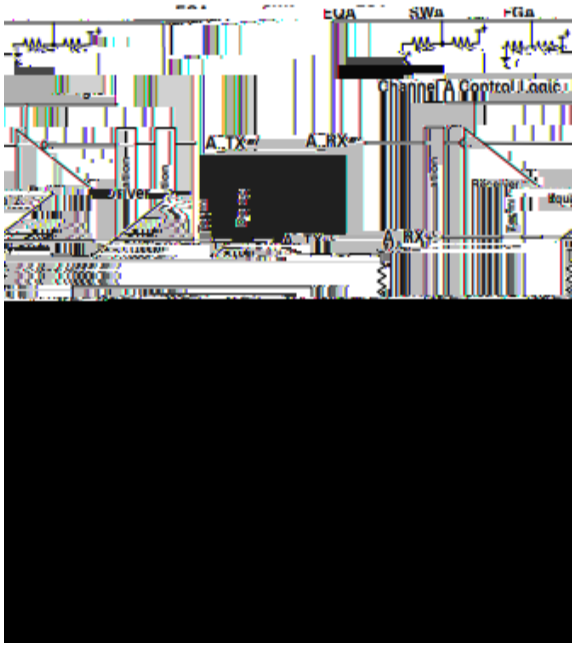
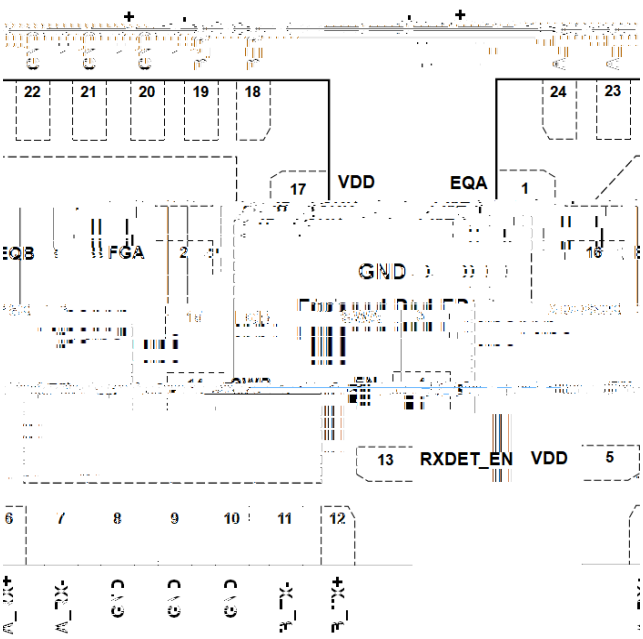

EQA
SWa
FGa
Channel A Control Logic
A_TX+
A_RX+
Driver
A_RX-


22
21
20
19
18
24
23
17
VDD
EQA
1
EQB
FGA
2
GND
13
RXDET_EN
VDD
5
6
7
8
9
10
11
12

EQA/B are the selection pins for the equalization.

	@2.5 GHz	@5 GHz
L (Tie 0−Ω to GND)	5.0	9.9
R (Tie Rext to GND)	2.7	6.9
F (Leave Open)		

PD	67 kΩ to GND	High−Z
Unplug Mode	High−Z	40 kΩ to VDD
Low Power Slumber Mode	50 Ω to VDD	40 kΩ to VDD
Active	50 Ω to VDD	50 Ω to VDD

LOW “L” (Pin tied to Ground)	800
Rext “R” (68 kΩ tied from pin to Ground)	1200
Float “F” (Pin open)	1000 (Default)
HIGH “H” (Pin tied to VDD)	1100

Over operating free−air temperature range (unless otherwise noted)

Supply Voltage (Note 2)	V_{DD}	−0.5	4.6	V
Voltage range at any input or output terminal	Differential I/O	−0.5	V_{DD} + 0.5	V
	LVCMOS inputs	−0.5	V_{DD} + 0.5	V
Output Current		−25	+25	mA
[redacted]			1.2	W
[redacted]		−65	150	°C
[redacted]			125	°C
[redacted]			34	°C/W
[redacted]			265	°C

[redacted]ce. If any of these limits are exceeded, device functionality [redacted]

2. All voltage values are with respect to the GND terminals.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Over operating free−air temperature range (unless otherwise noted)

V_{DD}	Main power supply	3.0	3.3	3.6	V
T_A	Operating free−air temperature Industrial Temperature Range	−40		+85	°C
C_{AC}	AC coupling capacitor	75	100	265	nF

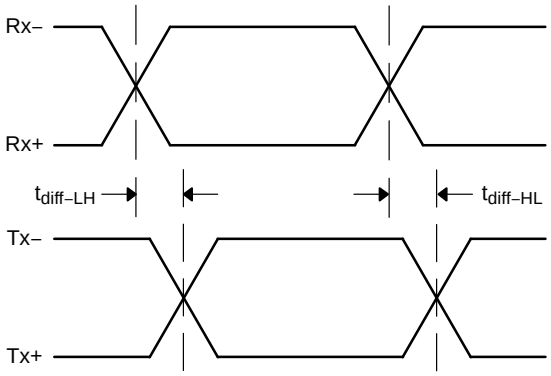
Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

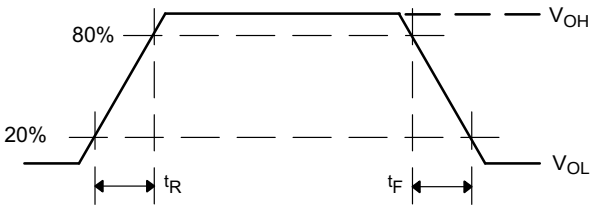
				(Note 4)		
VDD	Supply Voltage		3.0	3.3	3.6	V
IDD_{Active}	Active mode current	EN = 1, 10 Gbps, compliance test pattern		125	167	mA

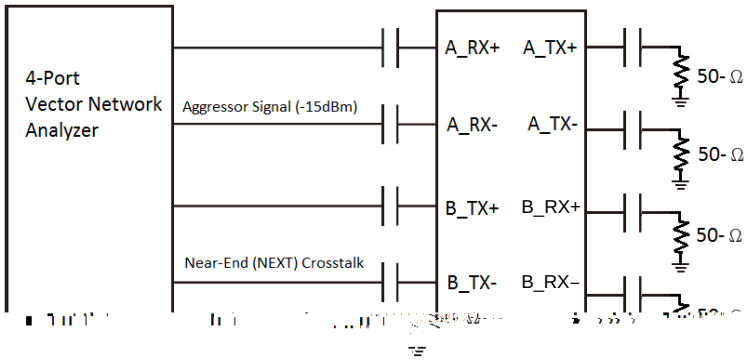
VDD = 3.3 V +/− 0.3 V Over operating free−air temperature range (unless otherwise noted)

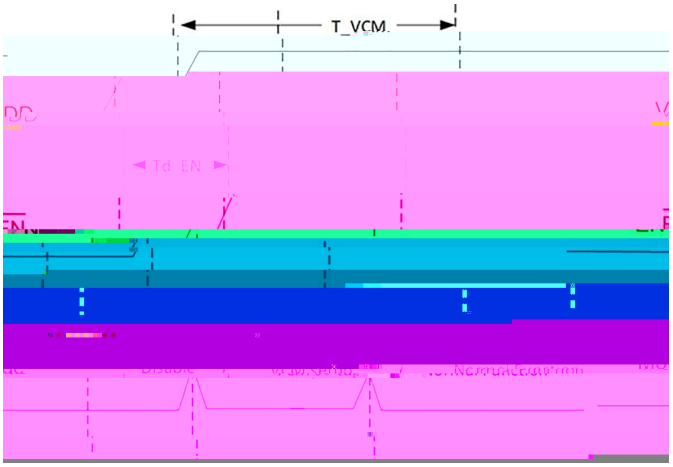
−

V_{IR}

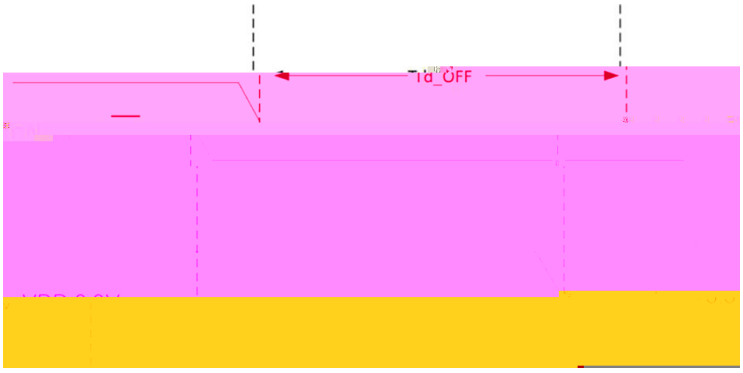

Rx–
Rx+
$t_{diff-LH}$
$t_{diff-HL}$
Tx–
Tx+


80%
20%
V_{OH}
V_{OL}
t_R
t_F


4-Port
Vector Network
Analyzer
Aggressor Signal (-15dBm)
Near-End (NEXT) Crosstalk
A_RX+
A_TX+
A_RX-
A_TX-
B_TX+
B_RX+
B_TX-
B_RX–
50- Ω
50- Ω
50- Ω



Td_EN	VDD to Enable Assertion timing requirement	Figure 6.	0			ms
T_VCM	Stabilization time for VCM	Figure 6.		330	400	ms

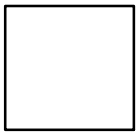


Td_OFF	Delay time required from EN de−assertion until VDD is powered off	Figure 7.	900			ms

Supply Voltage	3.3 V nominal, (3.0 V to 3.6 V)
Operation Mode (Control Pin Selection)	Floating by Default, adjust for application losses
TX AC Coupling Capacitors	220 nF nominal, 75 nF to 265 nF, see Figure 8
RX AC Coupling Capacitors	330 – 470 nF nominal, see Figure 8
Power Supply Capacitors	100 nF to GND close to each VCC pin, and 10 mF to GND on the VCC plane
Trace loss of FR4 before NB7NPQ1402E2M (Note 10)	Up to 11 dB Losses
Trace loss of FR4 after NB7NPQ1402E2M (Note 10)	Up To 3 dB Losses. Keep as short as possible for best performance.
Linear Range at 5 GHz	900 mV differential
DC Flat Gain Options	−1.2 dB, −0.2 dB, +0.8 dB, +1.8 dB
Equalization Options	6.9 to 12.1 dB
Differential Trace Impedance	90 Ω ±10%

10. Trace loss of FR4 was estimated to have 1 dB of loss per 1 inch of FR4 length with matched impedance and no VIAS.

UQFN24 2.5x2.5, 0.35P



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