Figure 1. Logic Diagram

Figure 2. X2QFN34 Package

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
14	CTRL_D0	LVCMOS INPUT	Pin D0 for control of Equalization settings on Channel D having internal 100 kΩ pull up and 200 kΩ pull down. 4 state input: HIGH “H” where pin is connected to V_{CC}, LOW “L” where pin is connected to Ground, FLOAT “F” where the pin is left floating (open) and Rext “R” where an external resistor 68 kΩ connected from pin to Ground. Refer Table 2 for the different settings.
15	CTRL_D1	LVCMOS INPUT	Pin D1 for control of Flat Gain settings on Channel D having internal 100 kΩ pull up and 200 kΩ pull down. 4 state input: HIGH “H” where pin is connected to V_{CC}, LOW “L” where pin is connected to Ground, FLOAT “F” where the pin is left floating (open) and Rext “R” where an external resistor 68 kΩ connected from pin to Ground. Refer Table 2 for the different settings.
16, 33	GND	GROUND	Reference Ground. GND pins must be externally connected to ground to guarantee proper operation.
18	D_RX+	DIFF INPUT	Channel D Differential input for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
19	D_RX−		
20	C_TX+	DIFF OUTPUT	Channel C Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
21	C_TX−		
23	CTRL_B0	LVCMOS INPUT	Pin B0 for control of Flat Gain settings on Channel B having internal 100 kΩ pull up and 200 kΩ pull down. 4 state input: HIGH “H” where pin is connected to V_{CC}, LOW “L” where pin is connected to Ground, FLOAT “F” where the pin is left floating (open) and Rext “R” where an external resistor 68 kΩ connected from pin to Ground. Refer Table 2 for the different settings.
24	CTRL_B1	LVCMOS INPUT	Pin B1 for control of Equalization settings on Channel B having internal 100 kΩ pull up and 200 kΩ pull down. 4 state input: HIGH “H” where pin is connected to V_{CC}, LOW “L” where pin is connected to Ground, FLOAT “F” where the pin is left floating (open) and Rext “R” where an external resistor 68 kΩ connected from pin to Ground. Refer Table 2 for the different settings.
25	B_RX+	DIFF INPUT	Channel B Differential input for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
26	B_RX−		
27	A_TX+	DIFF OUTPUT	Channel A Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled.
28	A_TX−		
31	CTRL_A0	LVCMOS INPUT	Pin A0 for control of Equalization settings on Channel A having internal 100 kΩ pull up and 200 kΩ pull down. 4 state input: HIGH “H” where pin is connected to V_{CC}, LOW “L” where pin is connected to Ground, FLOAT “F” where the pin is left floating (open) and Rext “R” where an external resistor 68 kΩ connected from pin to Ground. Refer Table 2 for the different settings.
32	CTRL_A1	LVCMOS INPUT	Pin A1 for control of Flat Gain settings on Channel A having internal 100 kΩ pull up and 200 kΩ pull down. 4 state input: HIGH “H” where pin is connected to V_{CC}, LOW “L” where pin is connected to Ground, FLOAT “F” where the pin is left floating (open) and Rext “R” where an external resistor 68 kΩ connected from pin to Ground. Refer Table 2 for the different settings.
EP	GND	GROUND	Exposed pad (EP). EP on the package bottom is thermally connected to the die for improved heat transfer out of the package. The pad is not electrically connected to the die, but is recommended to be soldered to GND on the PC Board.

DEVICE CONFIGURATION

Table 2. CONTROL PIN EFFECTS (Typical Values)

Settings	PORT A/B				PORT C/D				EQ (dB)	FG (dB)
	Channel A		Channel B		Channel C		Channel D			
	CTRL_A1 (FGA)	CTRL_A0 (EQA)	CTRL_B1 (EQB)	CTRL_B0 (FGB)	CTRL_C1 (EQC)	CTRL_C0 (FGC)	CTRL_D1 (FGD)	CTRL_D0 (EQD)		
1	L	L	L	L	L	L	L	L	10.9	−3
2	L	R	R	L	R	L	L	R	6.7	−3
3	L	F	F	L	F	L	L	F	8.9	−3
4	L	H	H	L	H	L	L	H	13.1	−3
5	R	L	L	R	L	R	R	L	10.9	−1.5
6	R	R	R	R	R	R	R	R	6.7	−1.5
7	R	F	F	R	F	R	R	F	8.9	−1.5
8	R	H	H	R	H	R	R	H	13.1	−1.5
9	F	L	L	F	L	F	F	L	10.9	0
10	F	R	R	F	R	F	F	R	6.7	0
11 (Default)	F	F	F	F	F	F	F	F	8.9	0
12	F	H	H	F	H	F	F	H	13.1	0
13	H	L	L	H	L	H	H	L	10.9	2
14	H	R	R	H	R	H	H	R	6.7	2
15	H	F	F	H	F	H	H	F	8.9	2
16	H	H	H	H	H	H	H	H	13.1	2

NOTE: EQ and FG can be set by adjusting the voltage to the control pins. There are 4 specific levels – HIGH “H” where pin is connected to V_{CC}, LOW “L” where pin is connected to Ground, FLOAT “F” where the pin is left floating (open) and Rext “R” where an external resistor 68 kΩ connected from pin to Ground. Please refer Table 7 for voltage levels.

Table 3. ATTRIBUTES

Parameter		
ESD Protection	Human Body Model Charged Device Model	≤ 2 kV ≤ 1.5 kV
Moisture Sensitivity, Indefinite Time Out of Dry pack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−O @ 0.125 in
Transistor Count		81,034
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch−up Test		

1. For additional information, see Application Note AND8003/D.

Table 4. ABSOLUTE MAXIMUM RATINGS Over operating free−air temperature range (unless otherwise noted)

Parameter	Description	Min	Max	Unit
Supply Voltage (Note 2)	V_{CC}	−0.5	4.6	V
Voltage range at any input or output terminal	Differential I/O	−0.5	V_{CC} + 0.5	V
	LVCMOS inputs	−0.5	V_{CC} + 0.5	V
Storage Temperature Range, T_{SG}		−65	150	°C
Maximum Junction Temperature, T_J			125	°C
Operating Ambient Temperature Range, T_A		−40	85	°C
Junction−to−Ambient Thermal Resistance @ 500 lfm, θ_{JA} (Note 3)			34	°C/W
Wave Solder, Pb−Free, T_{SOL}			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the

NB7NPQ7042M

PARAMETER MEASUREMENT DIAGRAMS

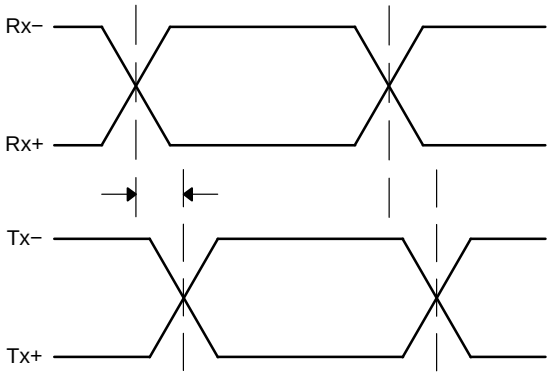


Figure 3. Propagation Delay

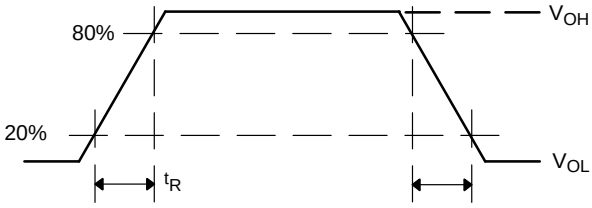
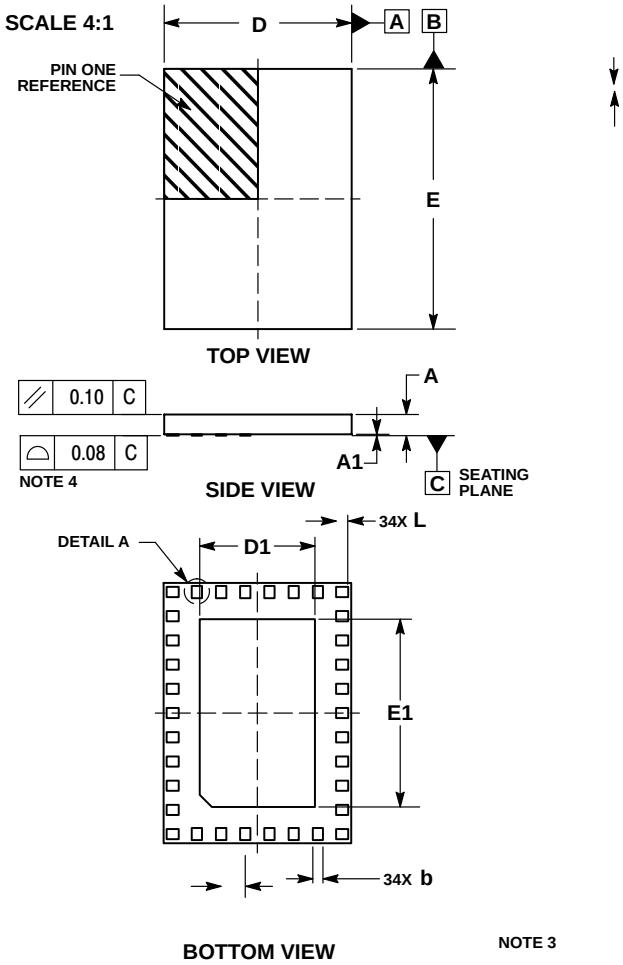


Figure 4. Output Rise and Fall Times

Table 11. DESIGN REQUIREMENTS

Design Parameter	Value

X2QFN34 3.1x4.3, 0.4P



DIM	MILLIMETERS	
	MIN	NOM
A		
A1	---	---
b		
D		
D1		
E		
E1		
e		
L		